

Compal Confidential

Model Name : A4WAB

File Name : LA-C341P

Compal Confidential

M/B Schematics Document

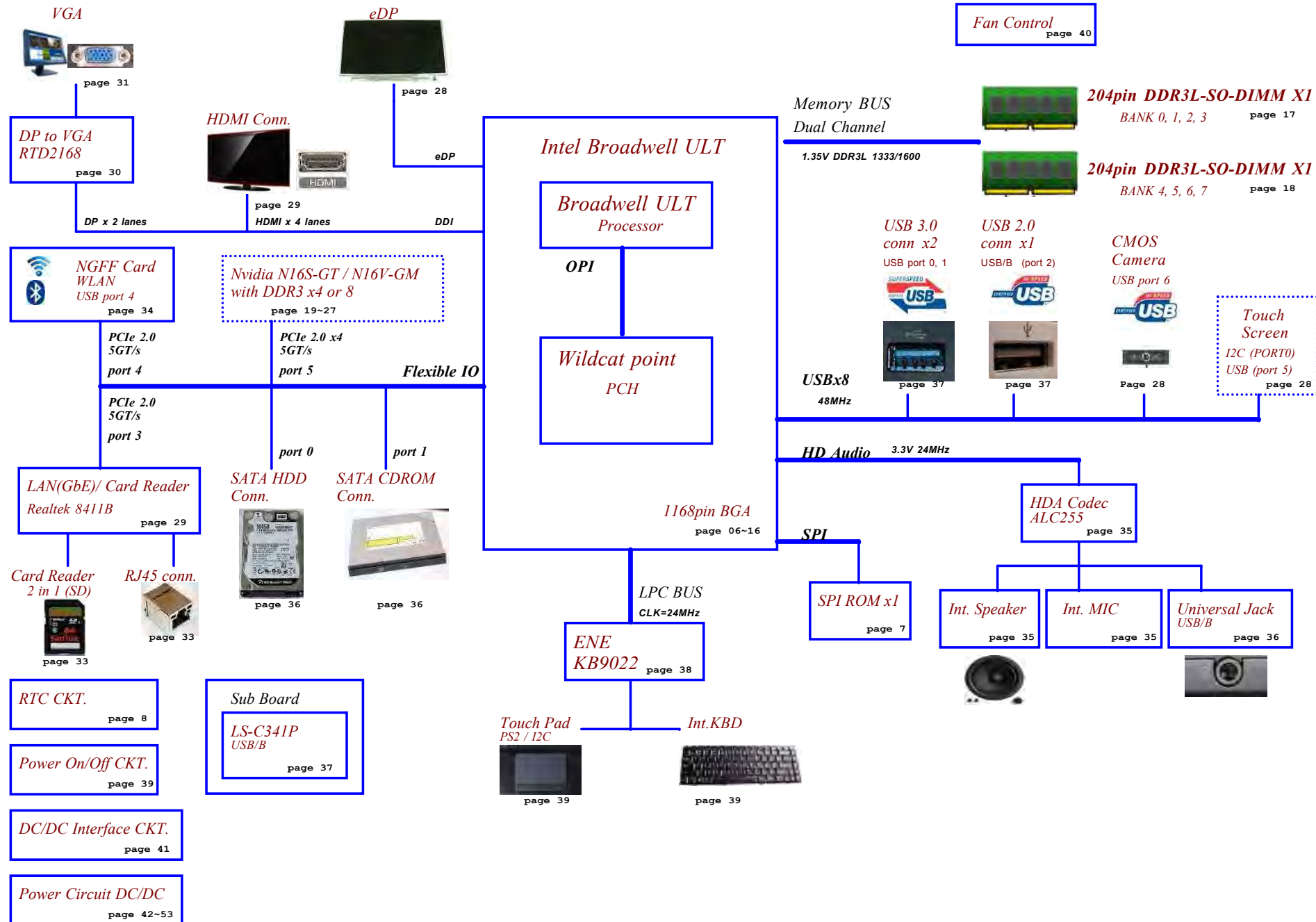
Intel Broadwell ULT (Broadwell + Wildcat point)

Nvidia N16S-GT / N16V-GM

2015-03-18

REV: 1 . 0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/09/16	Deciphered Date	2014/05/24	Cover Page	
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Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/09/16	Deciphered Date	2014/05/24	Block Diagrams	
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Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+0.675VS	+0.675VS power rail for DDR3L terminator	ON	OFF	OFF
+1.05VS_VTT	+1.05V power rail for CPU	ON	OFF	OFF
+1.05VSDGPU	+1.05VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+1.5VSDGPU	+1.5VSDGPU power rail for GPU	ON	OFF	OFF
+1.5VS	+1.5V power rail for CPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VLP	B+ to +3VLP power rail for suspend power	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU power rail for GPU	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	12K +/- 5%	0.347 V	0.354 V	0.360 V
2	15K +/- 5%	0.423 V	0.430 V	0.438 V
3	20K +/- 5%	0.541 V	0.550 V	0.559 V
4	27K +/- 5%	0.691 V	0.702 V	0.713 V
5	33K +/- 5%	0.807 V	0.819 V	0.831 V
6	43K +/- 5%	0.978 V	0.992 V	1.006 V
7	56K +/- 5%	1.169 V	1.185 V	1.200 V
8	75K +/- 5%	1.398 V	1.414 V	1.430 V
9	100K +/- 5%	1.634 V	1.650 V	1.667 V
10	130K +/- 5%	1.849 V	1.865 V	1.881 V
11	160K +/- 5%	2.015 V	2.031 V	2.046 V
12	200K +/- 5%	2.185 V	2.200 V	2.215 V
13	240K +/- 5%	2.316 V	2.329 V	2.343 V

USB 2.0	Port	3 External USB Port
EHCI1	0	USB Port (3.0 left front)
	1	USB Port (3.0 left back)
	2	USB Port(Right 2.0)
	3	
	4	Mini Card (WLAN+BT)
	5	Touch Screen
	6	Camera
7		
USB 3.0	Port	
XHCI	0	USB Port (3.0 left front)
	1	USB Port (3.0 Left back)
	2	
	3	

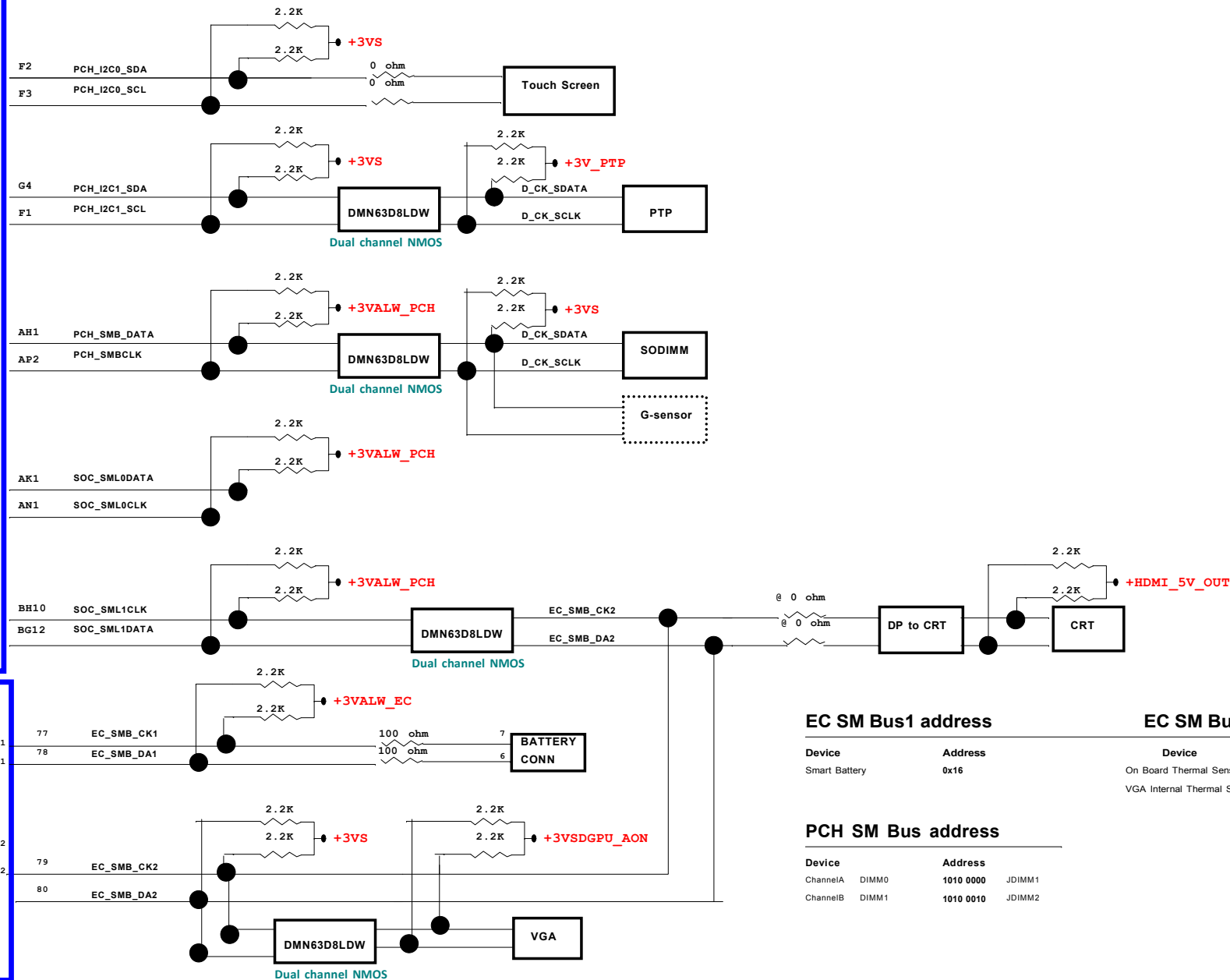
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	1.0
6	
7	

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
UMA Component	UMA@
GPU	VGA@
On Board HDD	HDD1@
Wire HDD	HDD2@
EMI Component	EMI@
EMI Reserve	XEMI@
ESD Component	ESD@
ESD Reserve	XESD@
TPM Module	TPM@
VRAM Selection	X76@
DGPU_IDEN	VGL@, VQMG@, SGT@
CPU_IDEN	HW@, BW@
GC6 2.0	GC6@
non GC6	NGC6@
EA40	1DMIC@
VA50	2DMIC@
Power BTN for debug	DB@
For 15" V3 series	V3@
G-Sensor	GSEN@

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SOC

KBC
KB9022



EC SM Bus1 address

Device	Address
Smart Battery	0x16

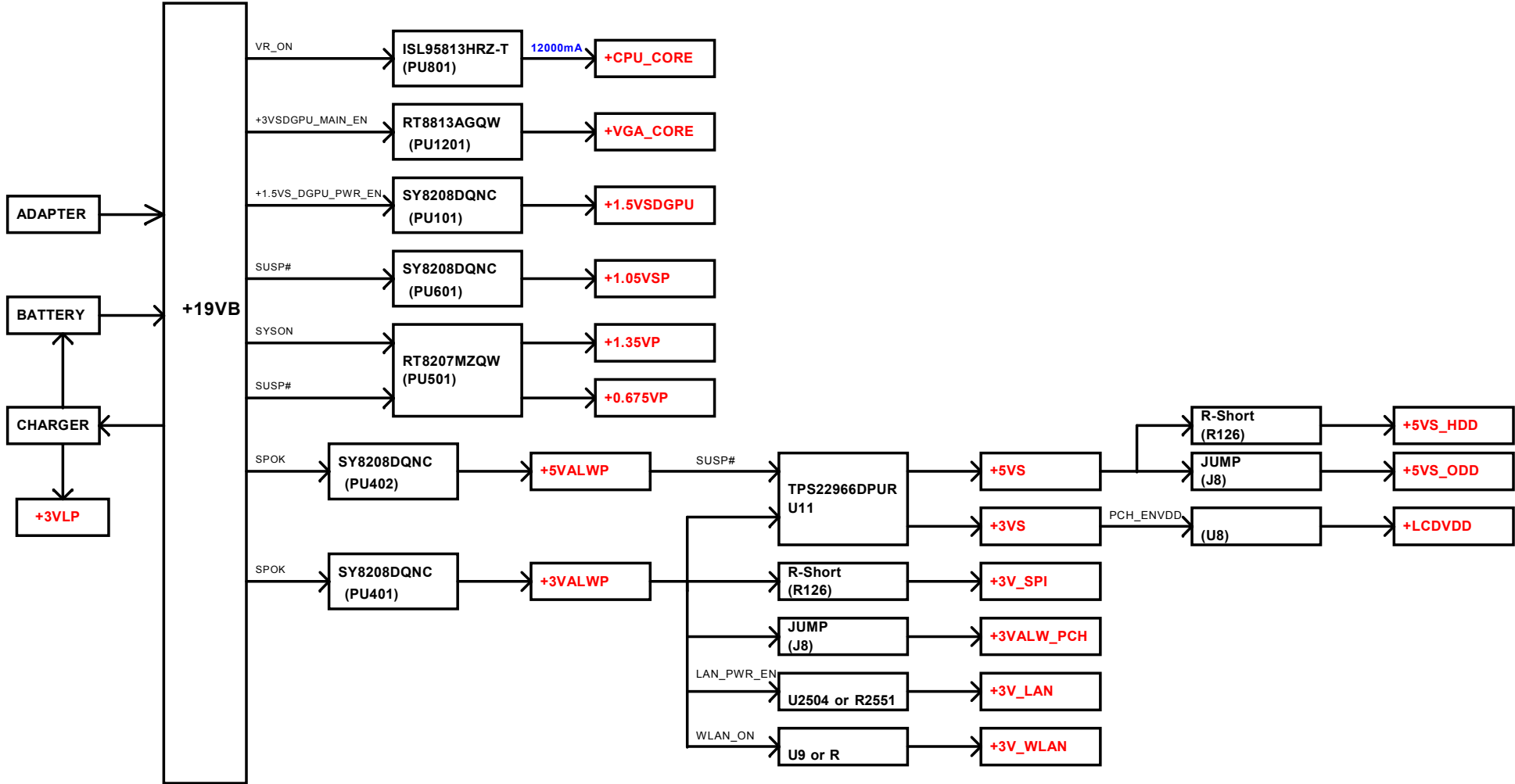
EC SM Bus2 address

Device	Address
On Board Thermal Sensor	0x96
VGA Internal Thermal Sensor	0x9E

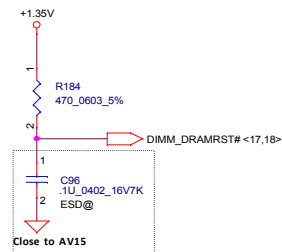
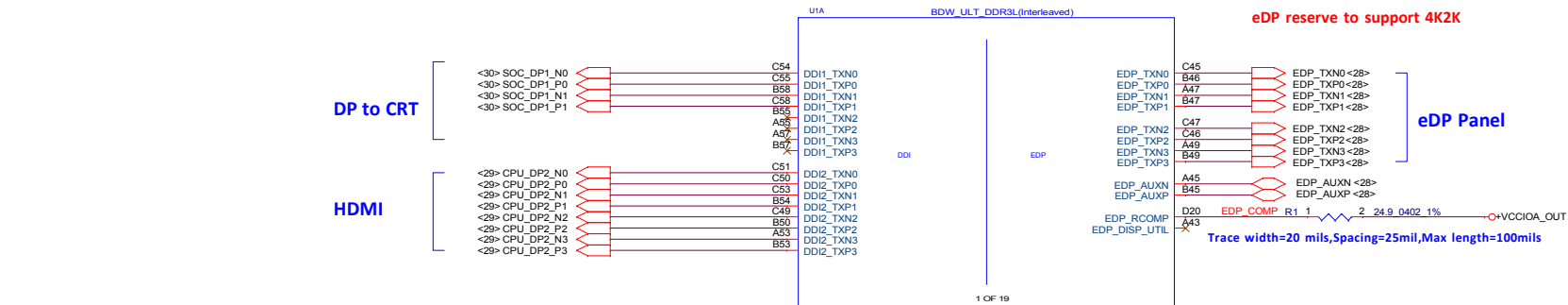
PCH SM Bus address

Device	Address
ChannelA DIMM0	1010 0000 JDIMM1
ChannelB DIMM1	1010 0010 JDIMM2

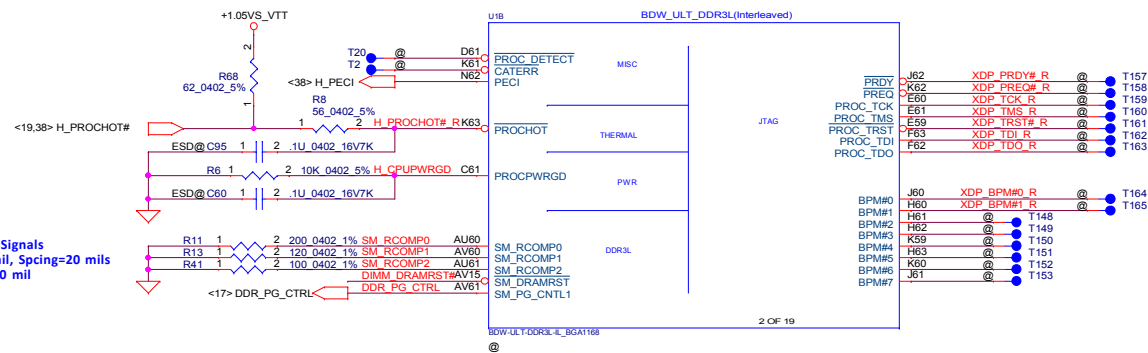
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Title	SMB/I2C
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DDR3 Compensation Signals
Trace width=12-15 mil, Spacing=20 mils
Max trace length= 500 mil



PCBA4WAB LA-C341PLS-C341P
DAZ1C700100

CPU_Boardwellintel QH1832.0G
QH18@
SA000083D40

CPU_Boardwellintel QH17152.0G
QH15@
SA000083C10

CPU_Boardwellintel QH15172.2G
QH15@
SA000083A10

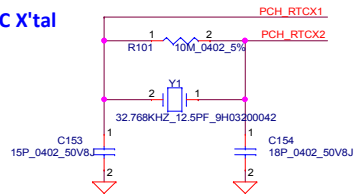
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SR244@
SA000083EB0

CPU_Boardwellintel SR23Y152.2G
SR23Y@
SA000089960

CPU_Boardwellintel SR23W172.4G
SR23W@
SA000089A70

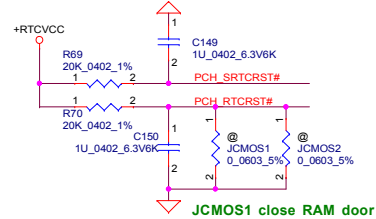
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Issued Date		2014/09/16	Deciphered Date		2014/05/24		
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RTC X'tal



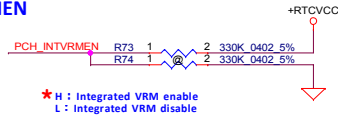
For BDW,
Crystal change to SJ10000LV00 (ESR=50K Ohm)

RTC Reset



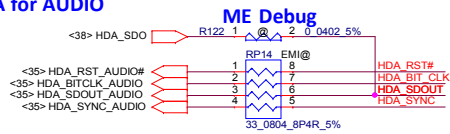
JCMOS1 close RAM door

INTVRMEN

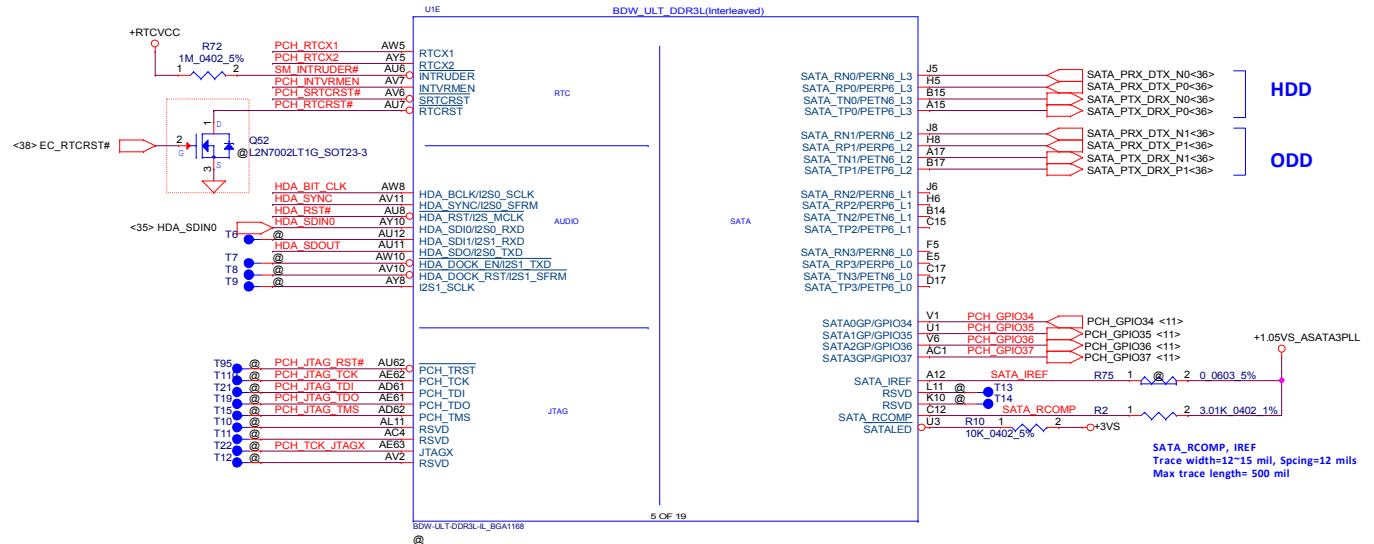
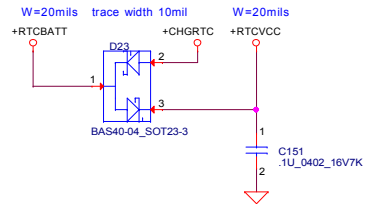


* H : Integrated VRM enable
L : Integrated VRM disable

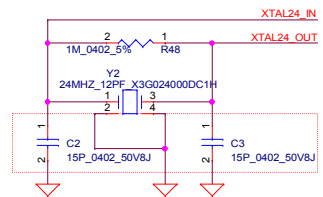
HDA for AUDIO



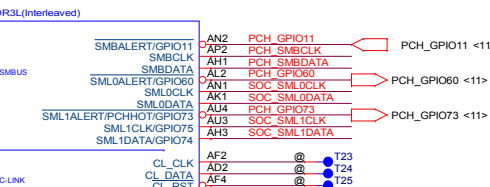
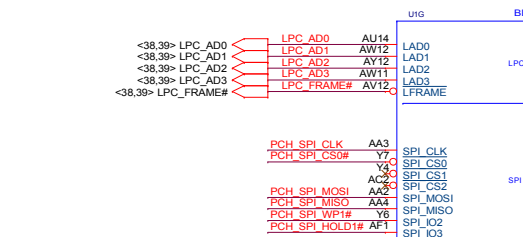
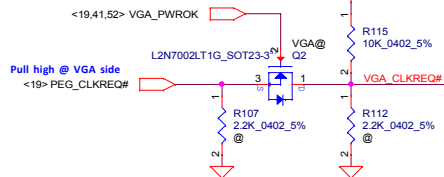
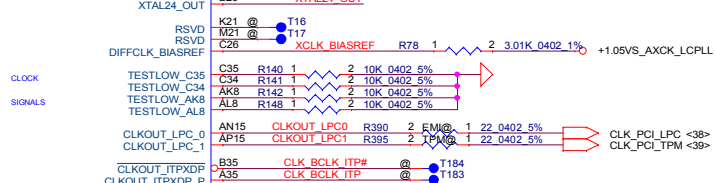
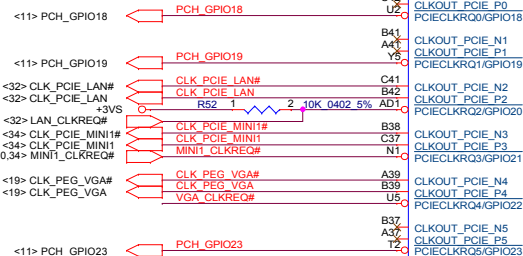
RTC Battery



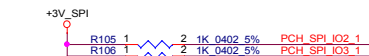
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/09/16	Deciphered Date	2014/05/24	BDW MCP(3/11) RTC,SATA,XDP	
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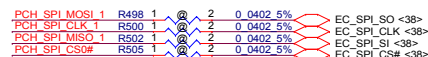
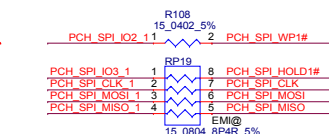
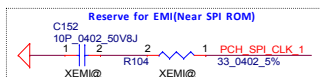
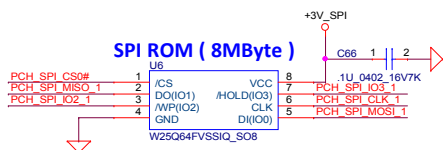
PCIE LAN WLAN VGA



SPI ROM

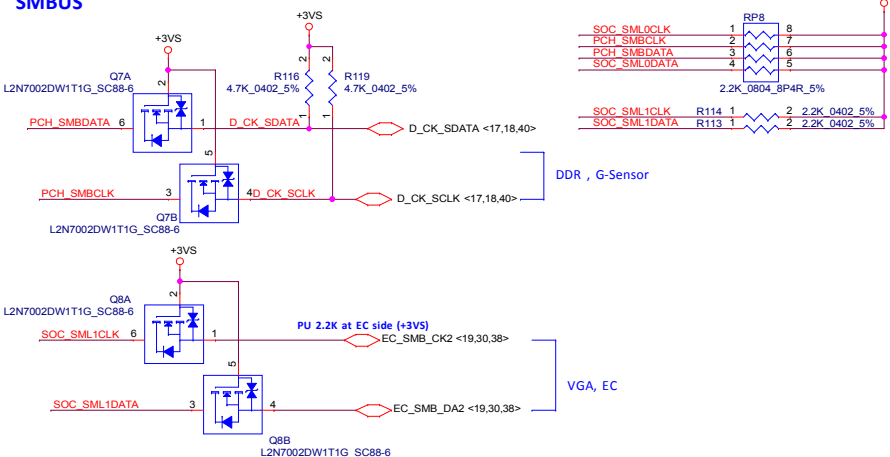


for Share EC ROM, +3VS
change to +3VALW



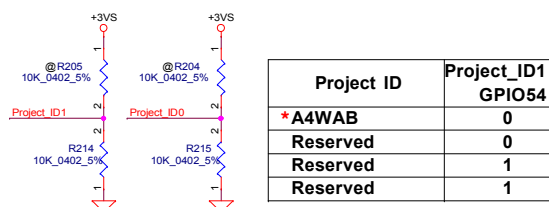
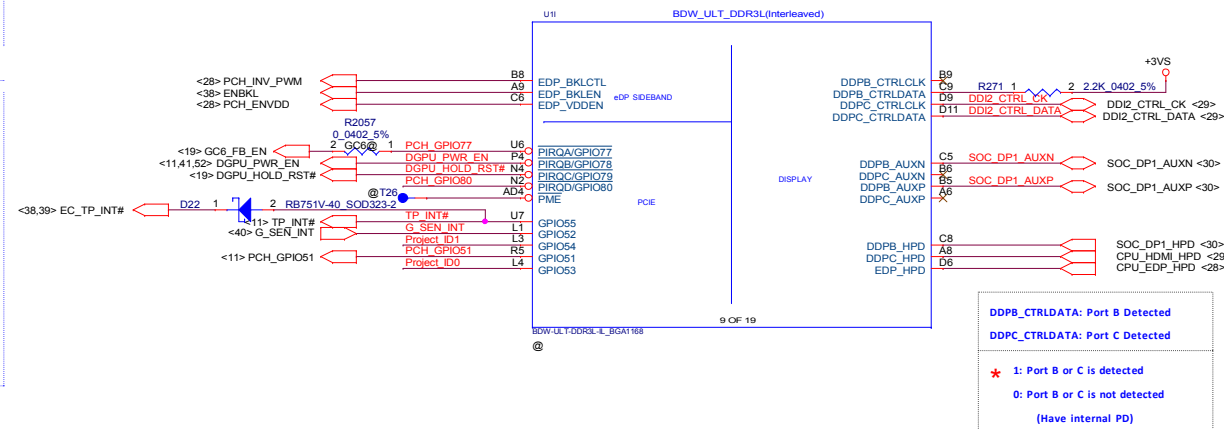
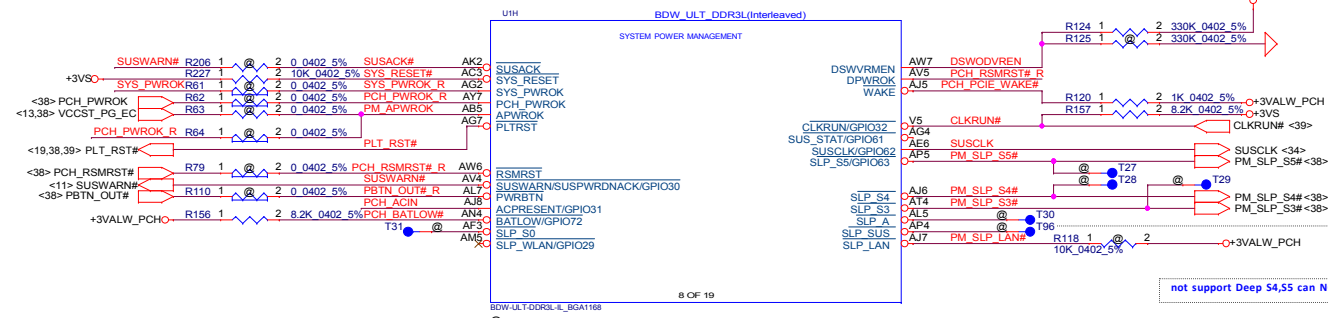
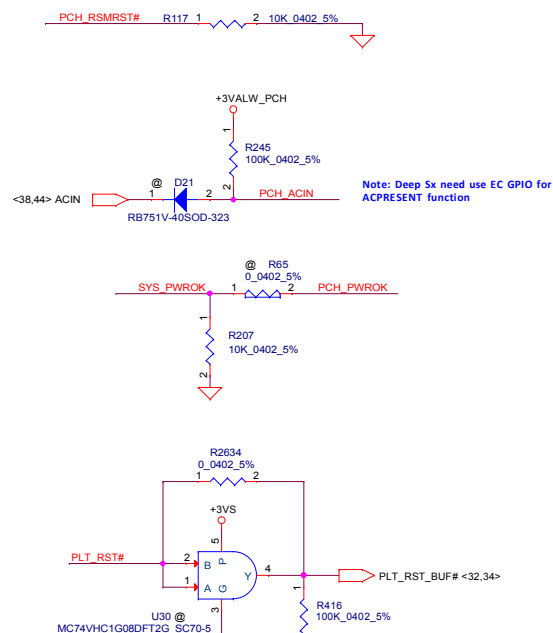
10/20: 2015 project not implement auto load,
change R498, R500, R502, R502 to non-pop.

SMBUS



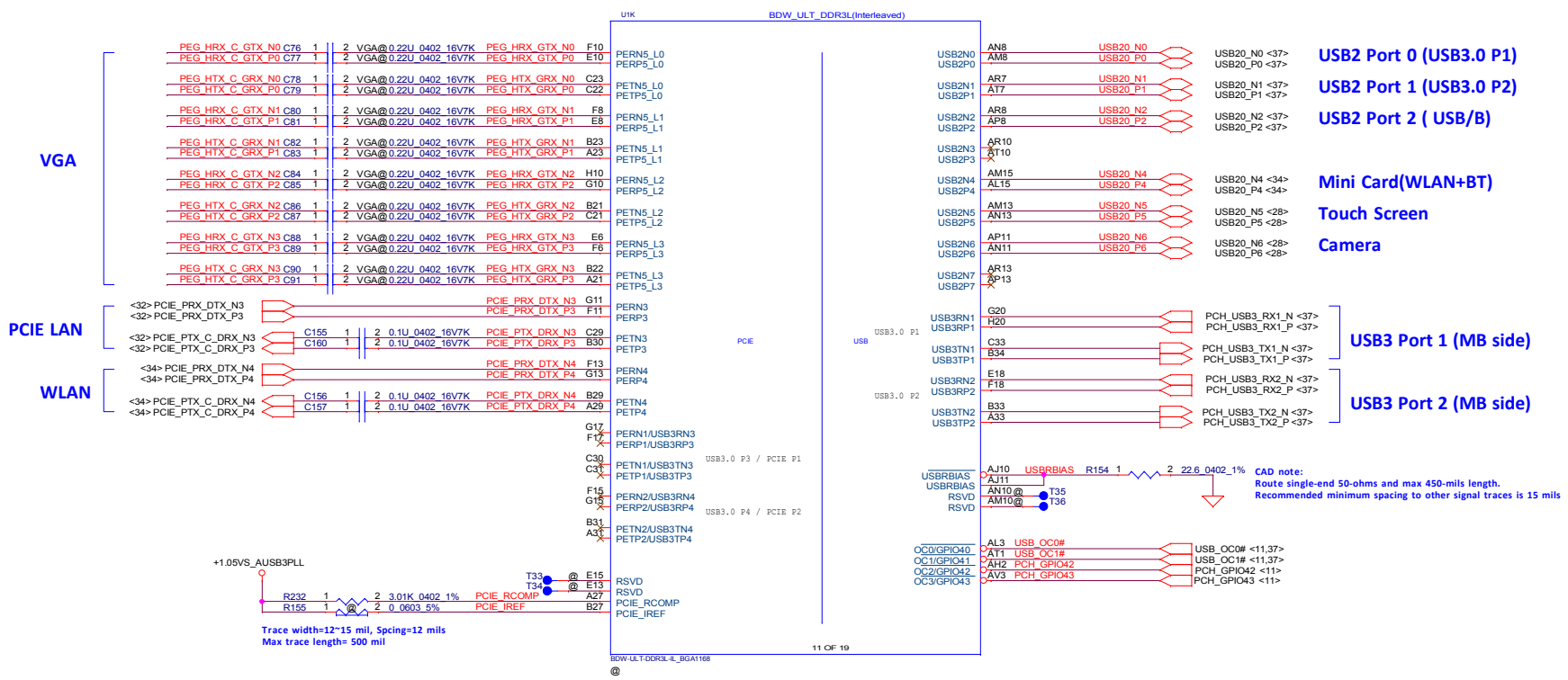
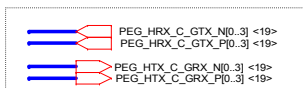
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				BDW MCP(4/1) CLK,SPI,SMBUS
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System Power Management

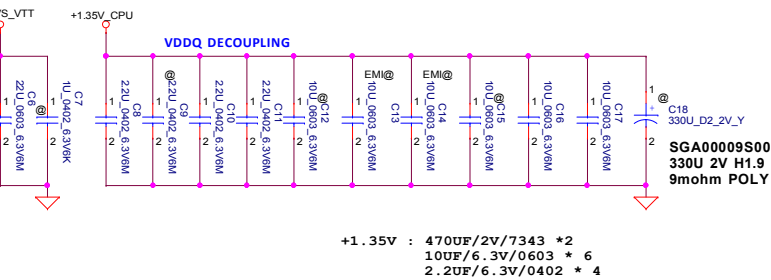
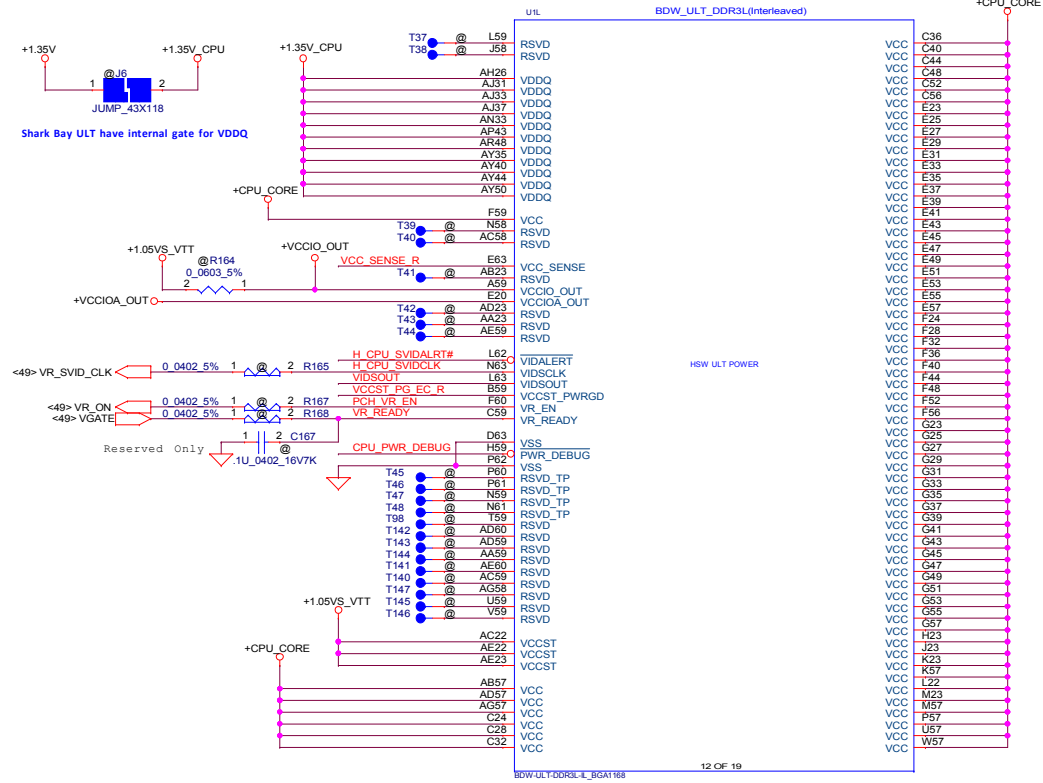
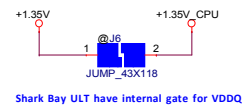
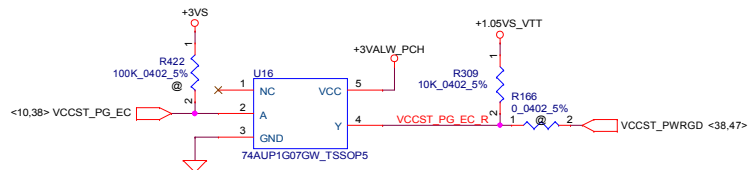
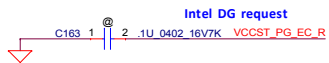
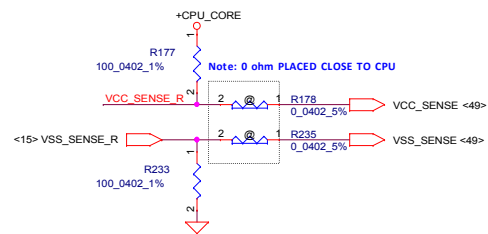
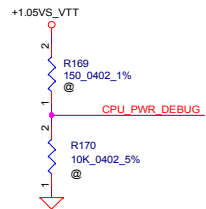
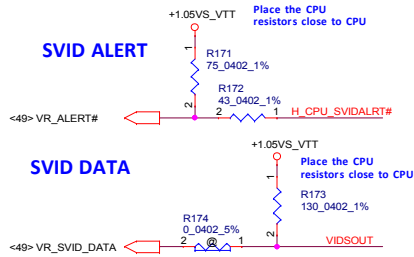


Project ID	Project_ID1 GPIO54	Project_ID0 GPIO53
* A4WAB	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

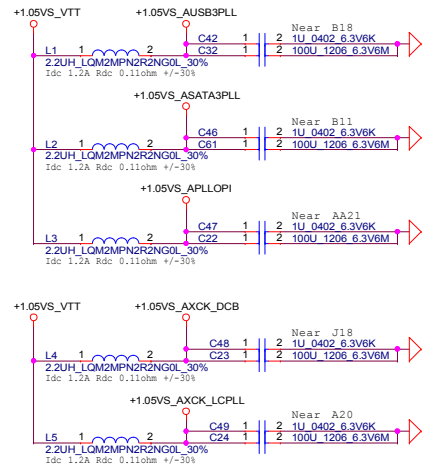
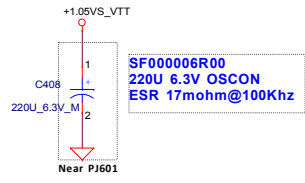
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Issued Date	2014/09/16	Deciphered Date	2014/05/24	Title	
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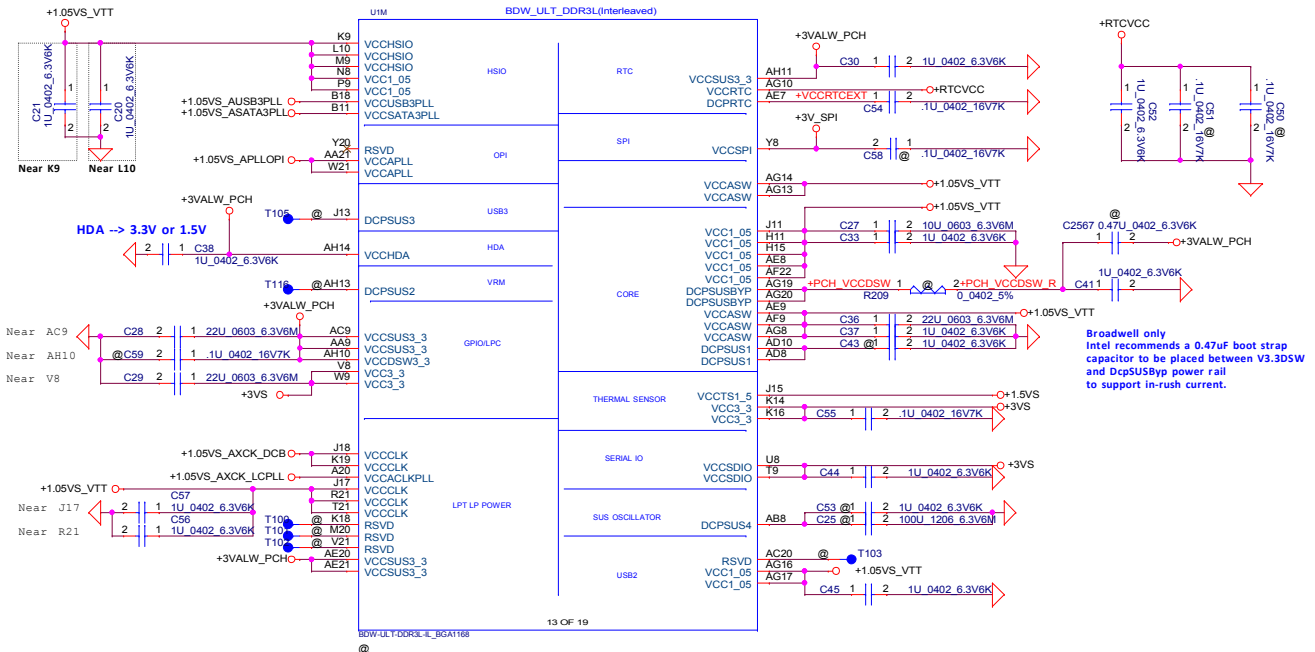
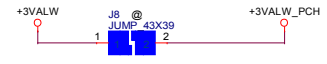
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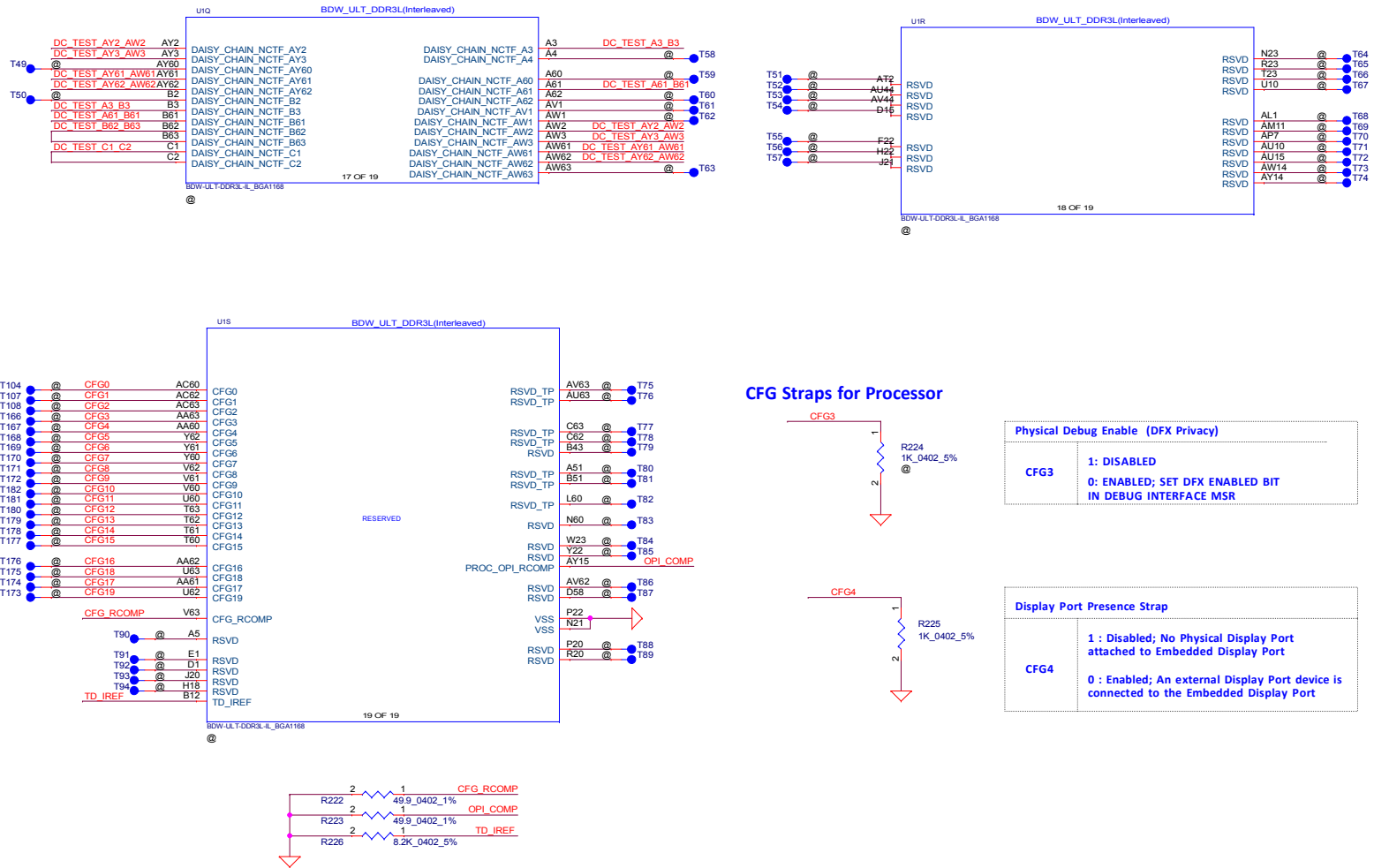


+3VALW TO +3VALW(PCH AUX Power)
Short J8 for PCH VCCSUS3.3

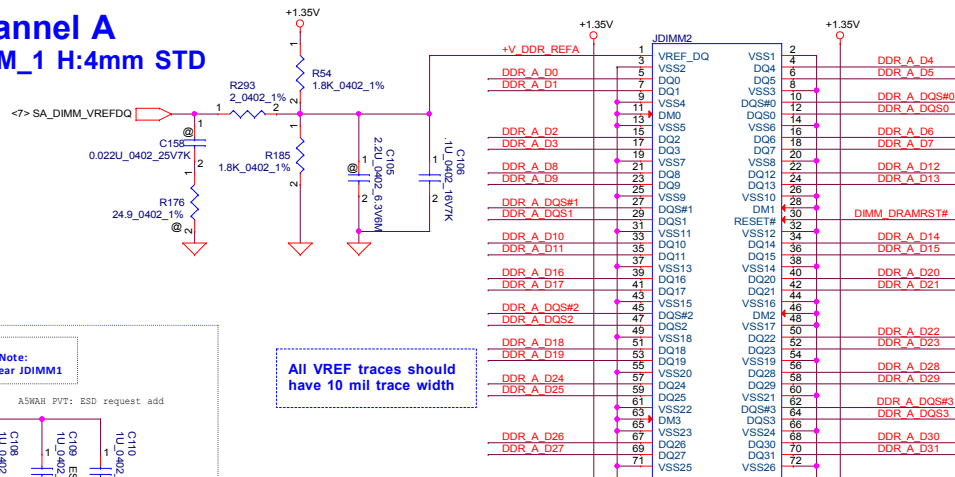


Broadwell only
 Intel recommends a 0.47uF boot strap
 capacitor to be placed between V3.3DSW
 and DcpSUSByP power rail
 to support in-rush current.

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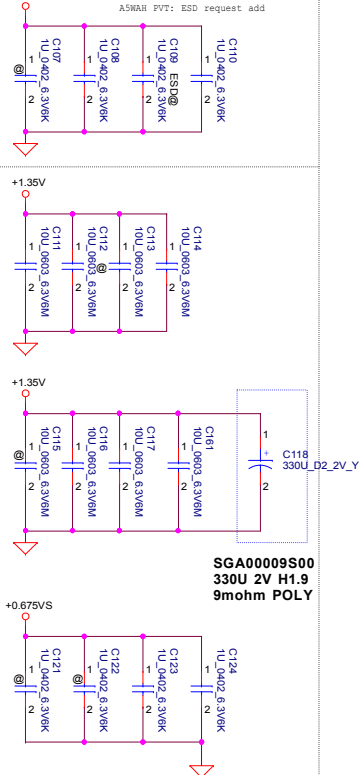


Channel A
DIMM_1 H:4mm STD



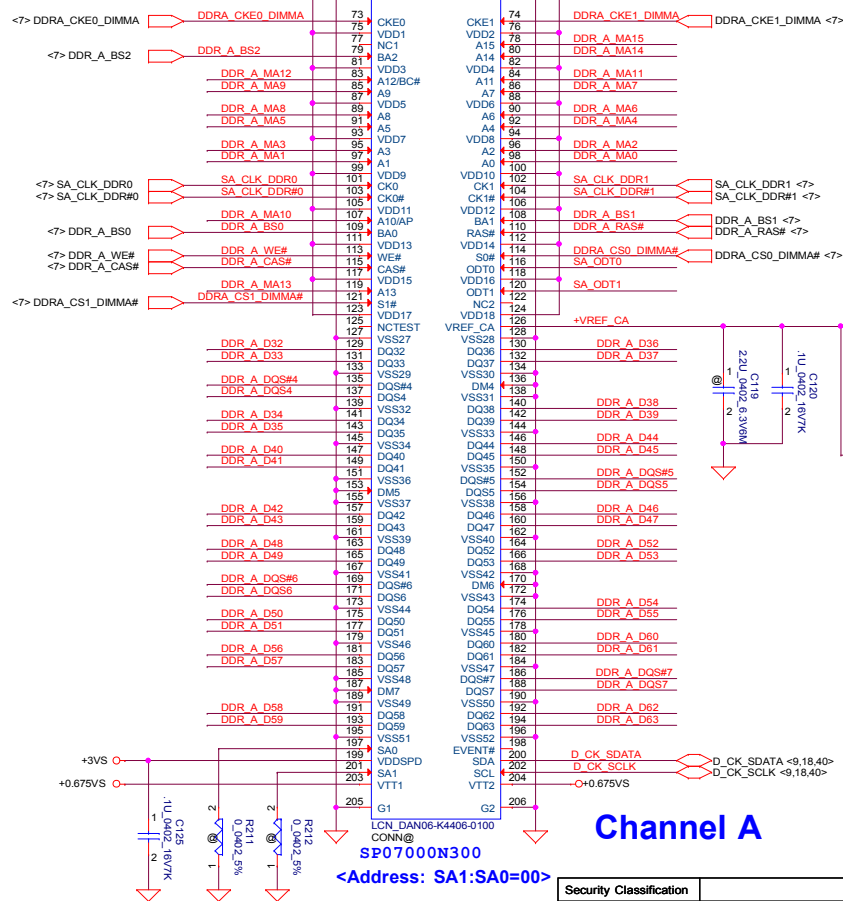
Layout Note:
Place near JDIMM1

All VREF traces should have 10 mil trace width

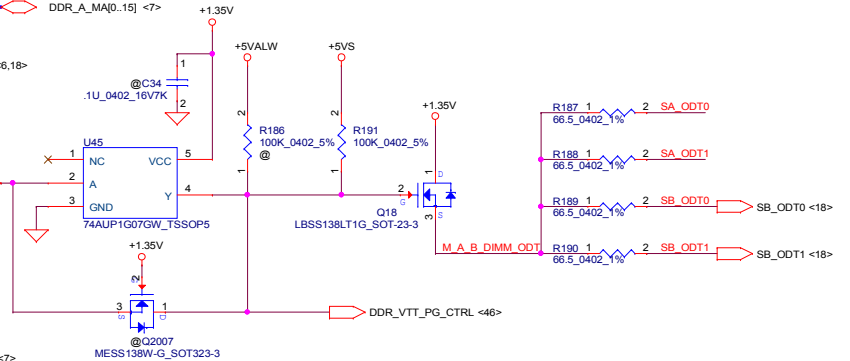


SGA00009S00
330U 2V H1.9
9mohm POLY

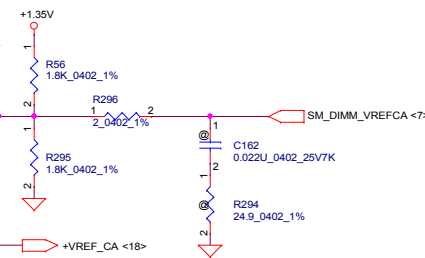
Layout Note:
Place near JDIMM1.203,204



Channel A



Reserve for cost test.

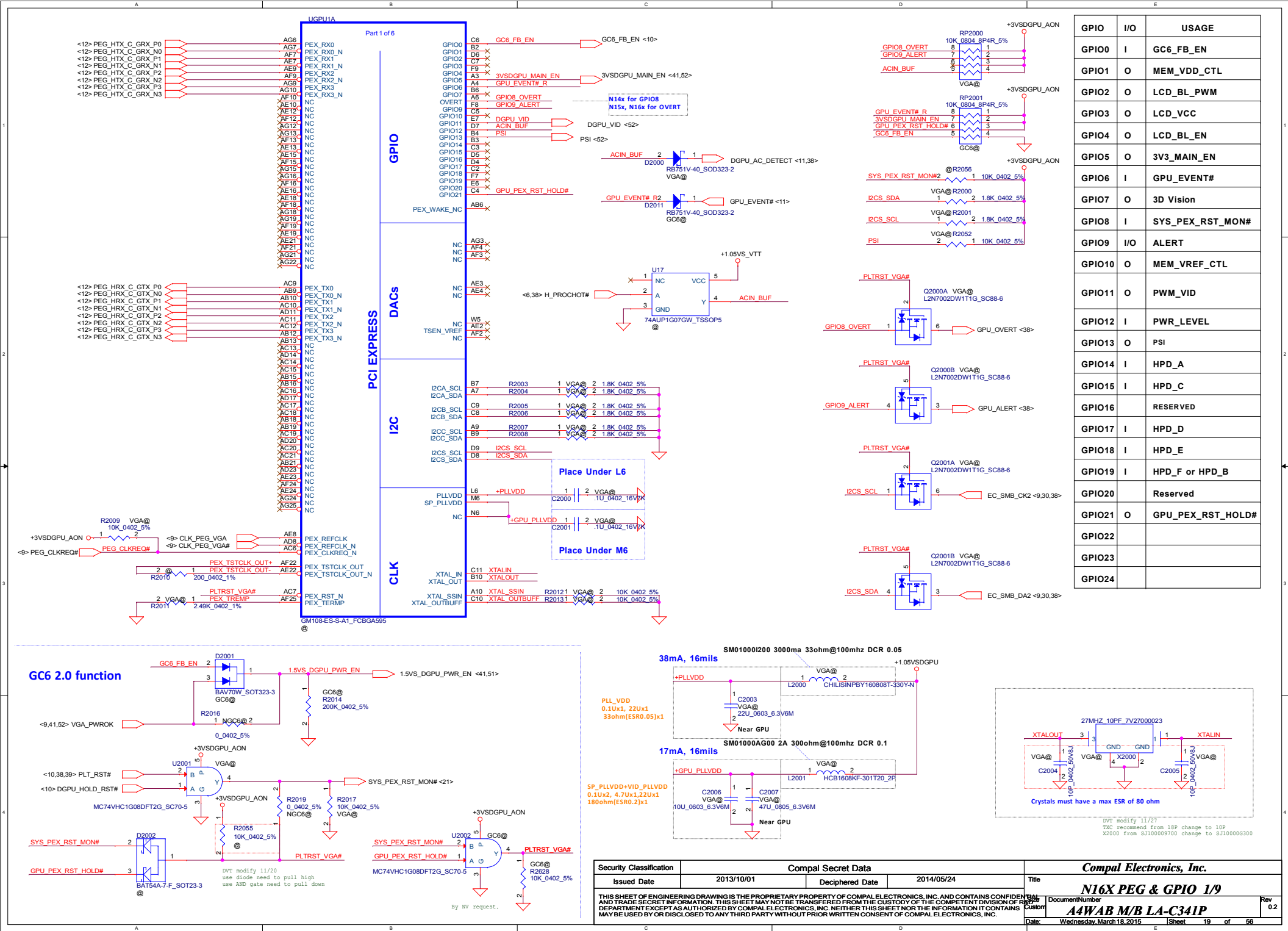


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Date:		Wednesday, March 18, 2015		Sheet	17 of 56

DIMM_2 H:4mm
Reverse

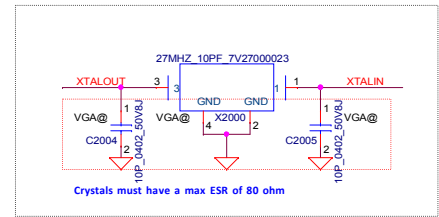
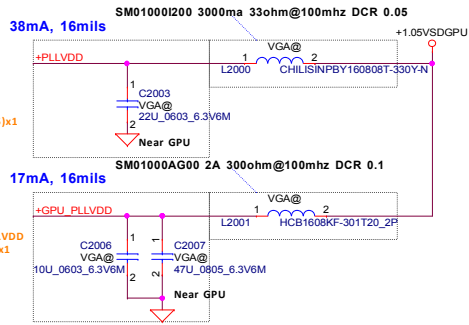
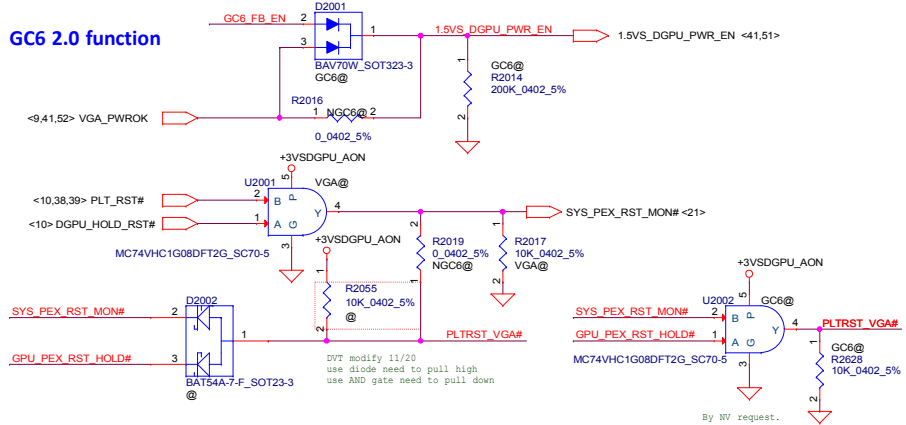


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GPIO	I/O	USAGE
GPIO0	I	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BL_EN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16		RESERVED
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		
GPIO24		

GC6 2.0 function



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VRAM Interface

UGPU1
N16S-GT
SGT@
SA000087F10

R3 P/N:

UGPU1
N16V-GM
VGM@
SA000088R20

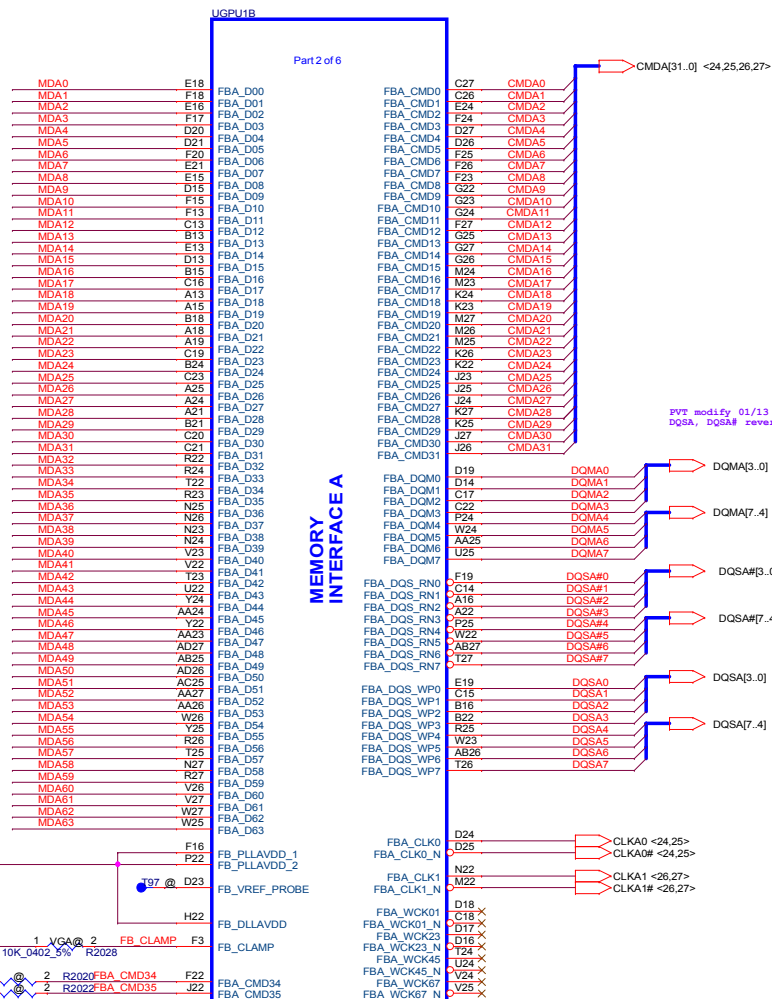
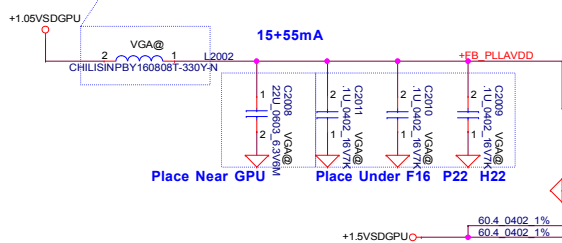
R3 P/N:

<24,25> MDA[15..0] MDA[15..0]
<24,25> MDA[31..16] MDA[31..16]
<26,27> MDA[47..32] MDA[47..32]
<26,27> MDA[63..48] MDA[63..48]

NV 15x DG-06803-V03
NV 16x DG-07158-V04

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB20 64	FBx_PL1_AVDD and FB_DLL_AVDD Combined	0.1 µF X7R 22 µF X5R	0402 0805	2 1	Under GPU Near GPU
		Bead Type			
		30 Ω (ESR=0.010 Ω)	0603	1	Near GPU

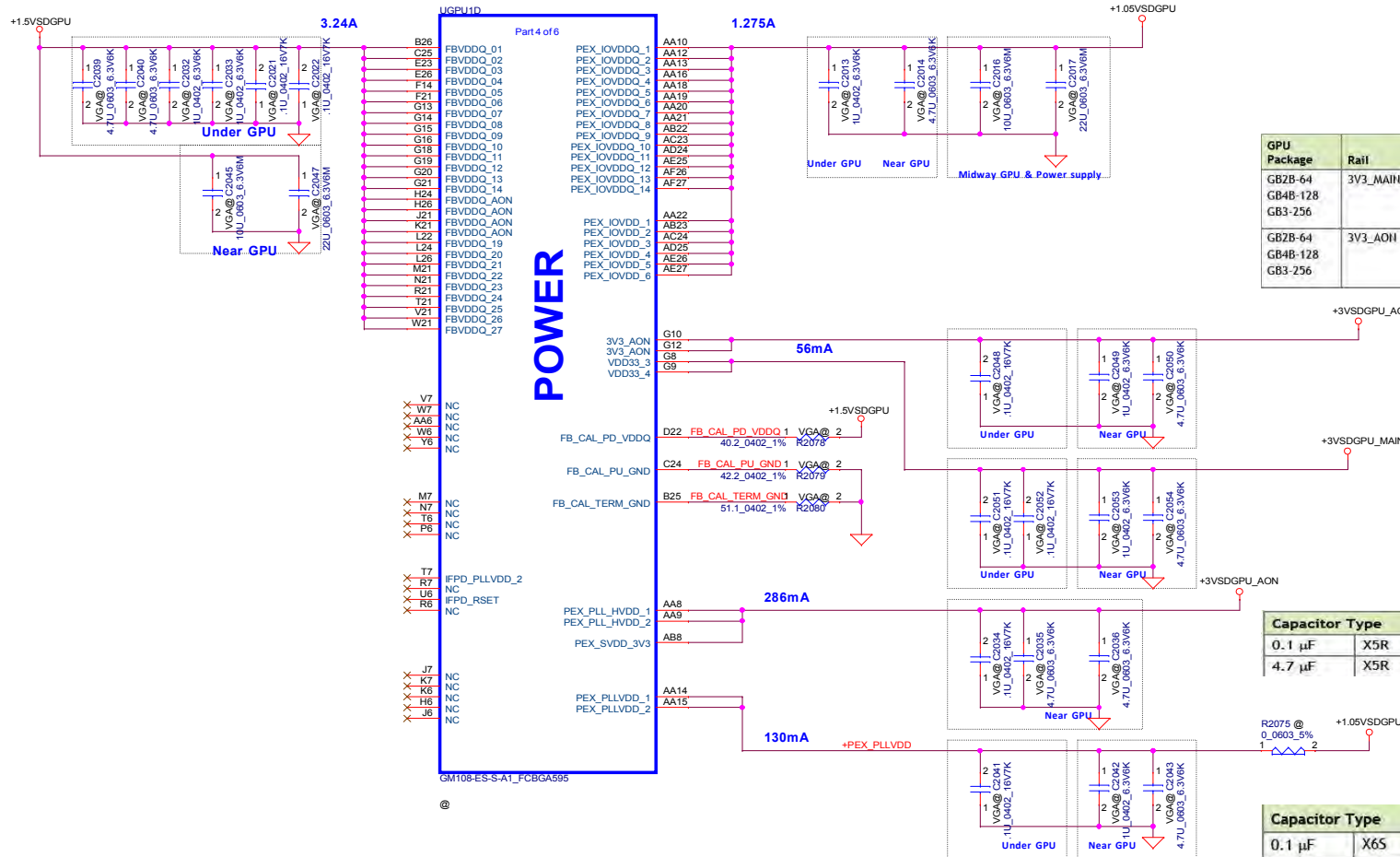
SM010001200 3000ma 33ohm@100mhz DCR 0.05



NV 15x DG-06803-V03
NV 16x DG-07158-V04

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64	0.1µF	X7R 0402	2	Under GPU
DDR3	1µF	X7R 0603	2	Under GPU
	4.7µF	X6S 0603	2	Under GPU
	10µF	X5R 0805	1	Near GPU
	22µF	X5R 0805	1	Near GPU

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64	1.0µF	X6S 0402	1	Under GPU
	4.7µF	X6S 0603	1	Near GPU
	10µF	X5R 0805	1	Midway between GPU and Power Supply
	22µF	X5R 0805	1	Midway between GPU and Power Supply

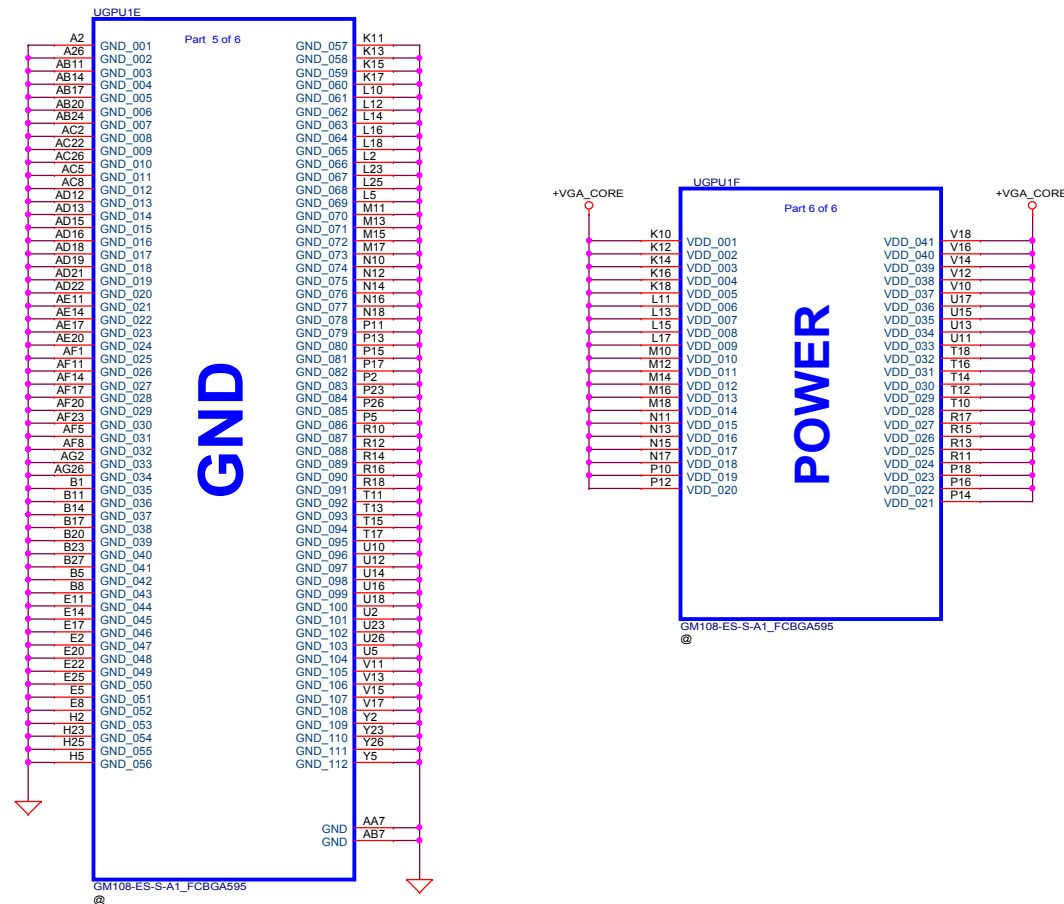


GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	3V3_MAIN	0.1µF	X6S 0402	2	Under GPU
GB4B-128		1µF	X5R 0603	1	Near GPU
GB3-256		4.7µF	X5R 0603	1	Near GPU
GB2B-64	3V3_AON	0.1µF	X6S 0402	1	Under GPU
GB4B-128		1µF	X5R 0603	1	Near GPU
GB3-256		4.7µF	X5R 0603	1	Near GPU

Capacitor Type	Footprint	Population	Location
0.1µF	X5R	0402	1
4.7µF	X5R	0603	2

Capacitor Type	Footprint	Population	Location
0.1µF	X6S	0402	1
1.0µF	X5R	0603	1
4.7µF	X5R	0805	1

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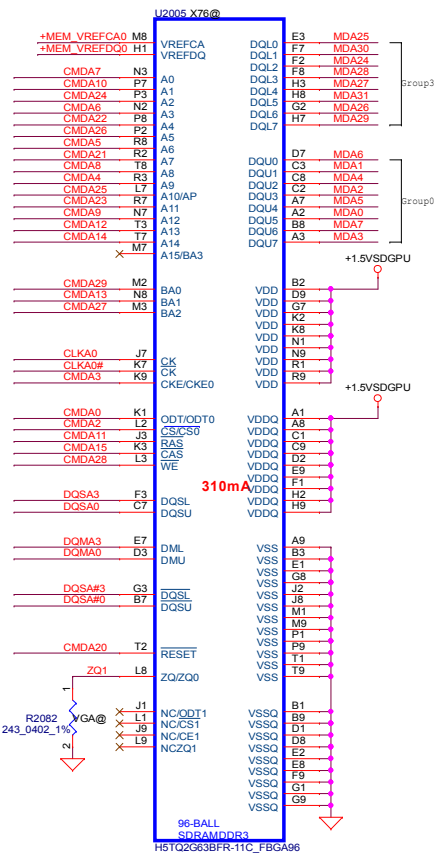
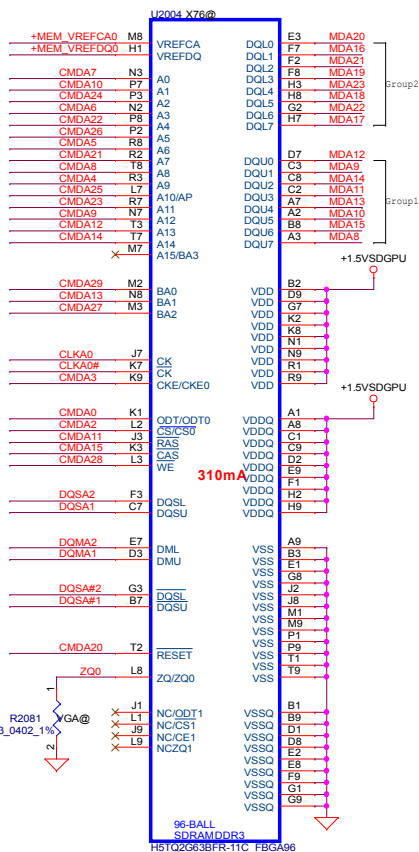


VRAM DDR3 chips

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 <20,25,26,27> DQSA[7..0] → DQSA[7..0]
 <20,25,26,27> DQMA[7..0] → DQMA[7..0]
 <20,25,26,27> MDA[63..0] → MDA[63..0]
 <20,25,26,27> CMDA[30..0] → CMDA[30..0]

Lower Rank 0 BOT SIDE

VRAM P/N: SA00006E840

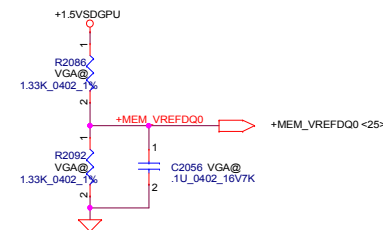
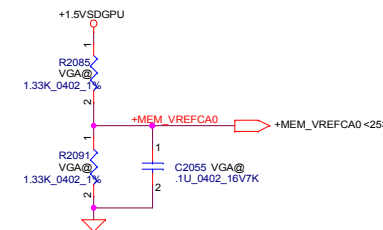
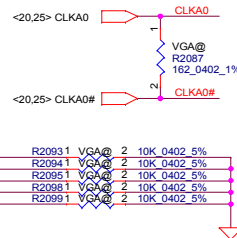
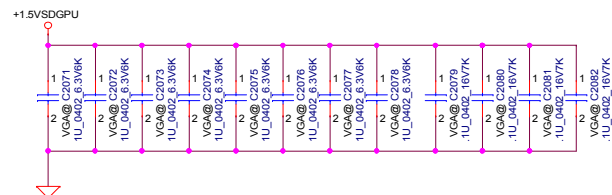


Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17			CS1*	
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

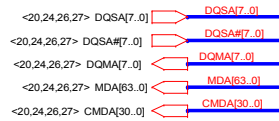
Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population		Location
FBVDD/Q Combined			FBVDDQ	FBVDD	
0.1 μF	X7R	0402	2		Under DRAM
1.0 μF	X7R	0603	4		Under DRAM
10 μF	X5R	0805	0		Close to DRAM

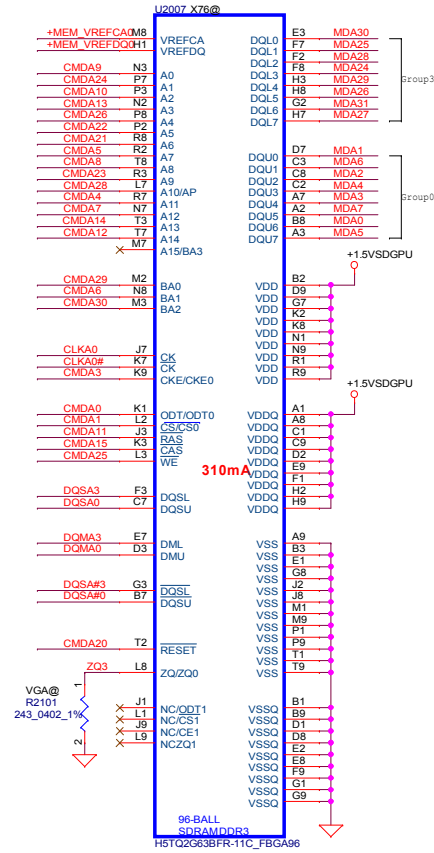
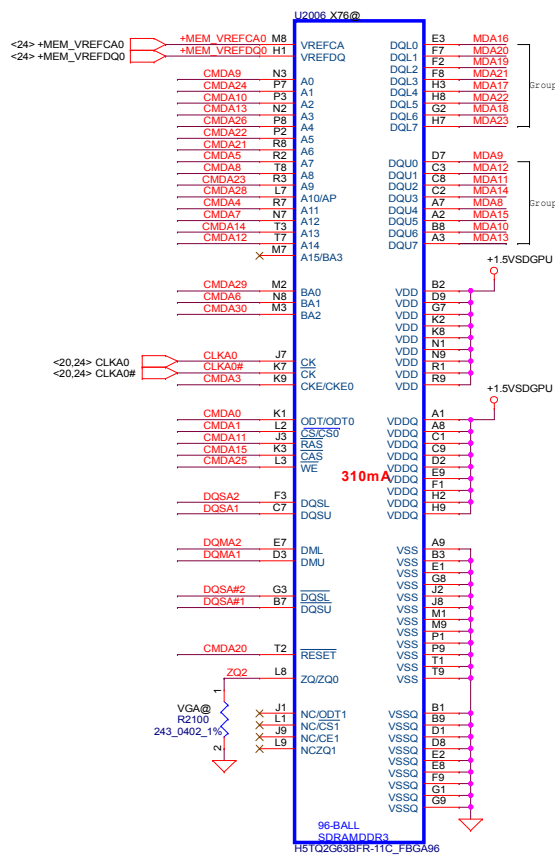


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VRAM DDR3 chips

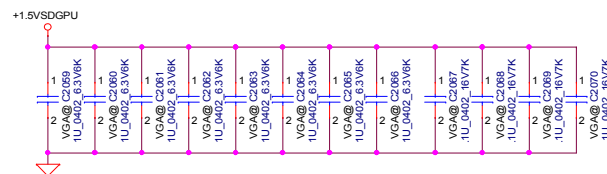


Lower Rank 1 TOP SIDE








Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

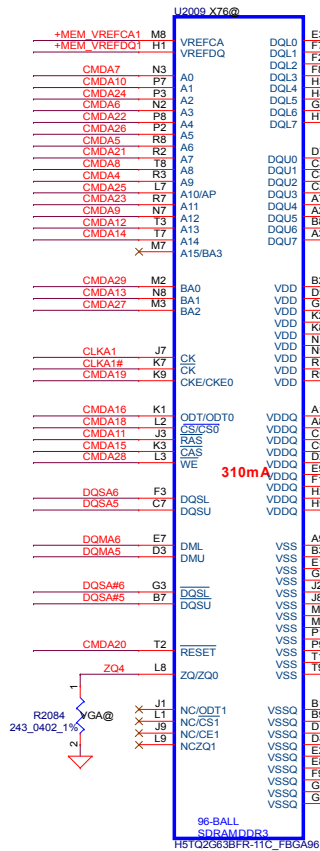
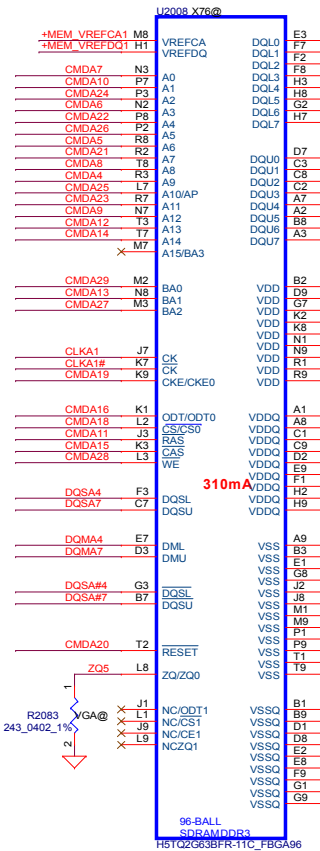


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VRAM DDR3 chips

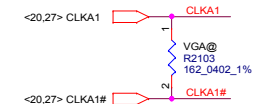
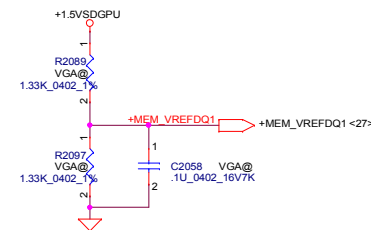
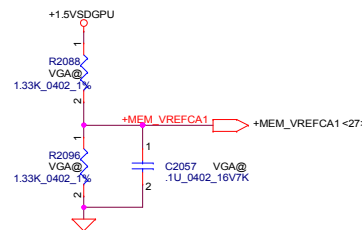
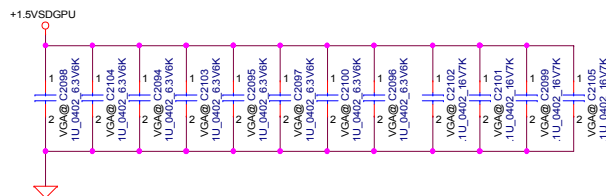
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 <20,24,25,27> DQMA [7..0]  DQMA [7..0]
 <20,24,25,27> MDA [63..0]  MDA [63..0]
 <20,24,25,27> CMDA [30..0]  CMDA [30..0]

Upper Rank 0 BOT SIDE



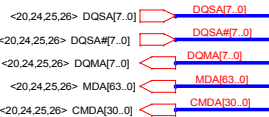
Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT	ODT	
CMD17			CS1*	
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

DDR3	Command Bit	Default Pull-down
	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

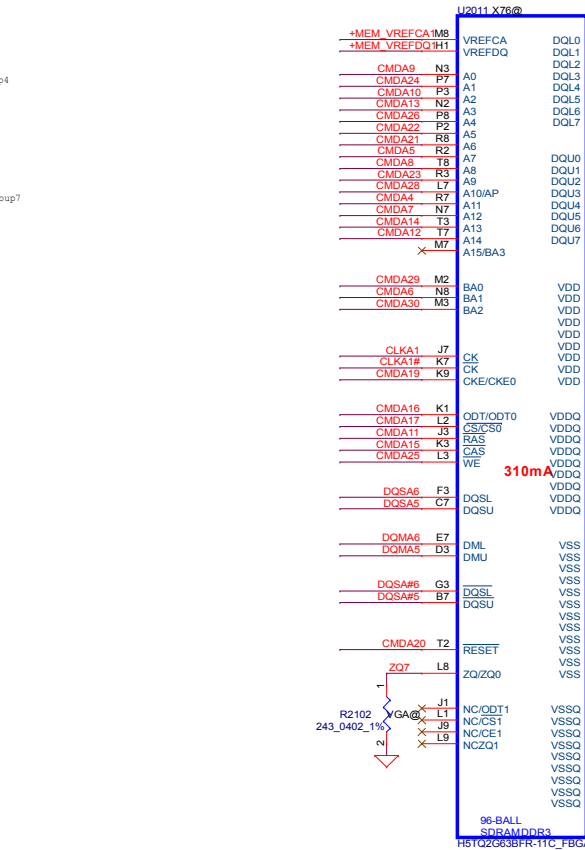
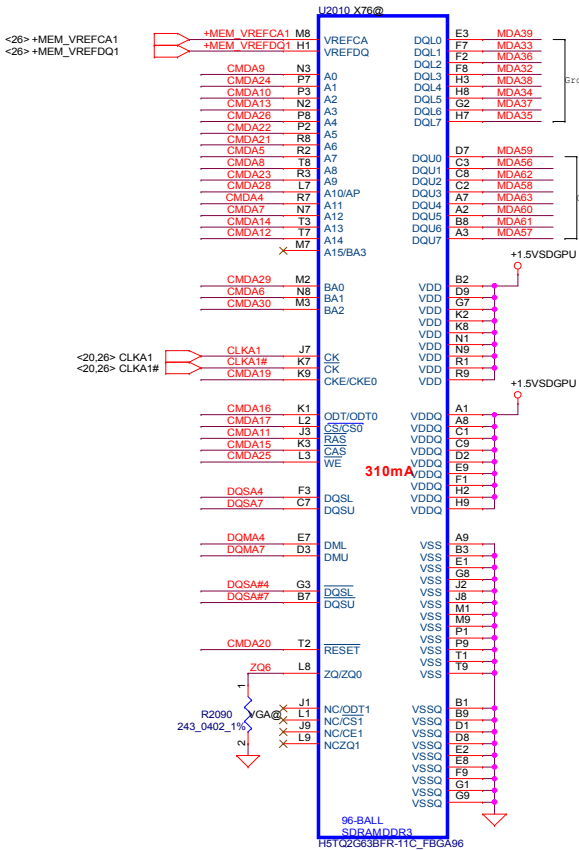


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VRAM DDR3 chips



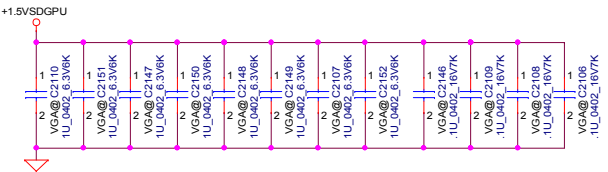
Upper Rank 1 TOP SIDE



ASMBUS SWAP

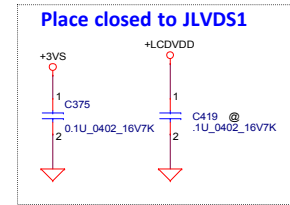
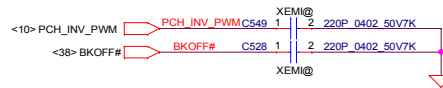
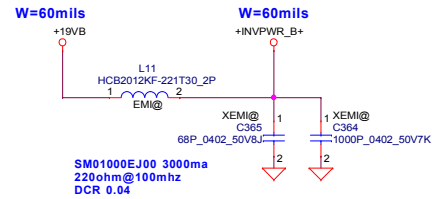
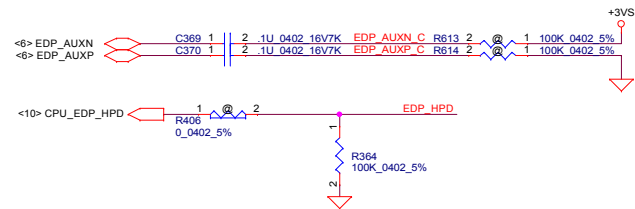
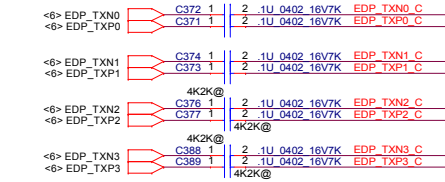
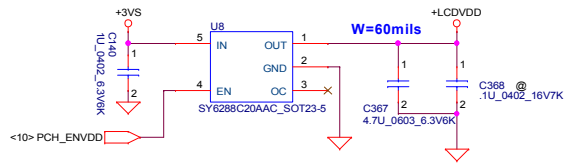
Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17			CS1*	
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

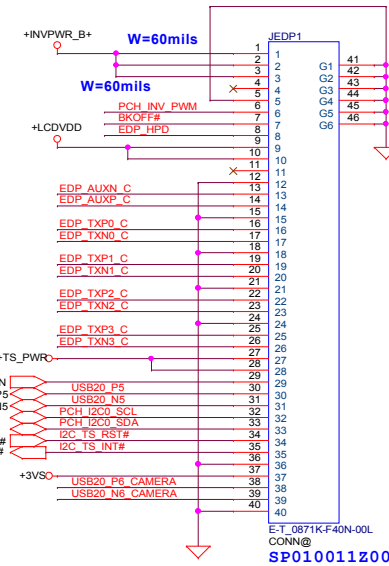


EDP / LVDS conn.

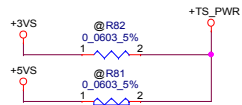
LCD POWER CIRCUIT



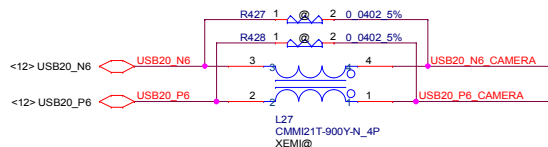
Follow A4QAS pin assignment
LCD/ LED PANEL Conn.



Touch Screen

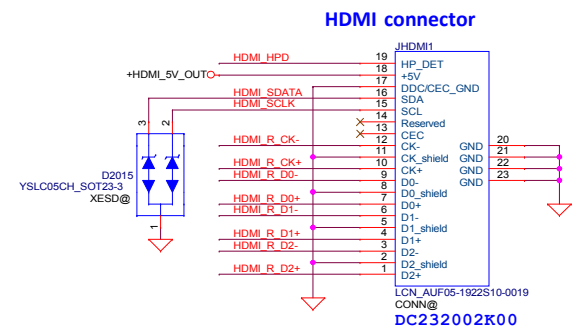
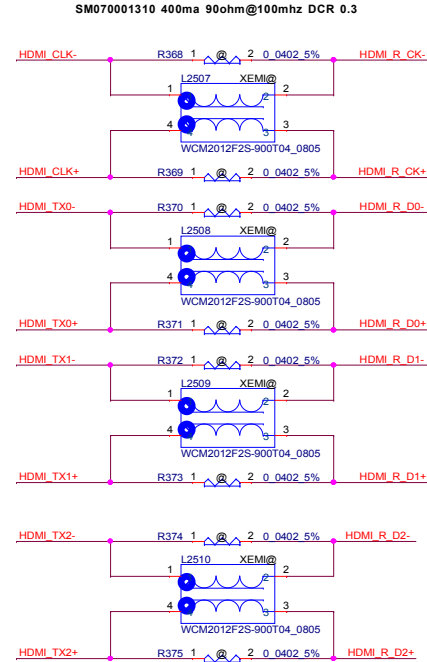
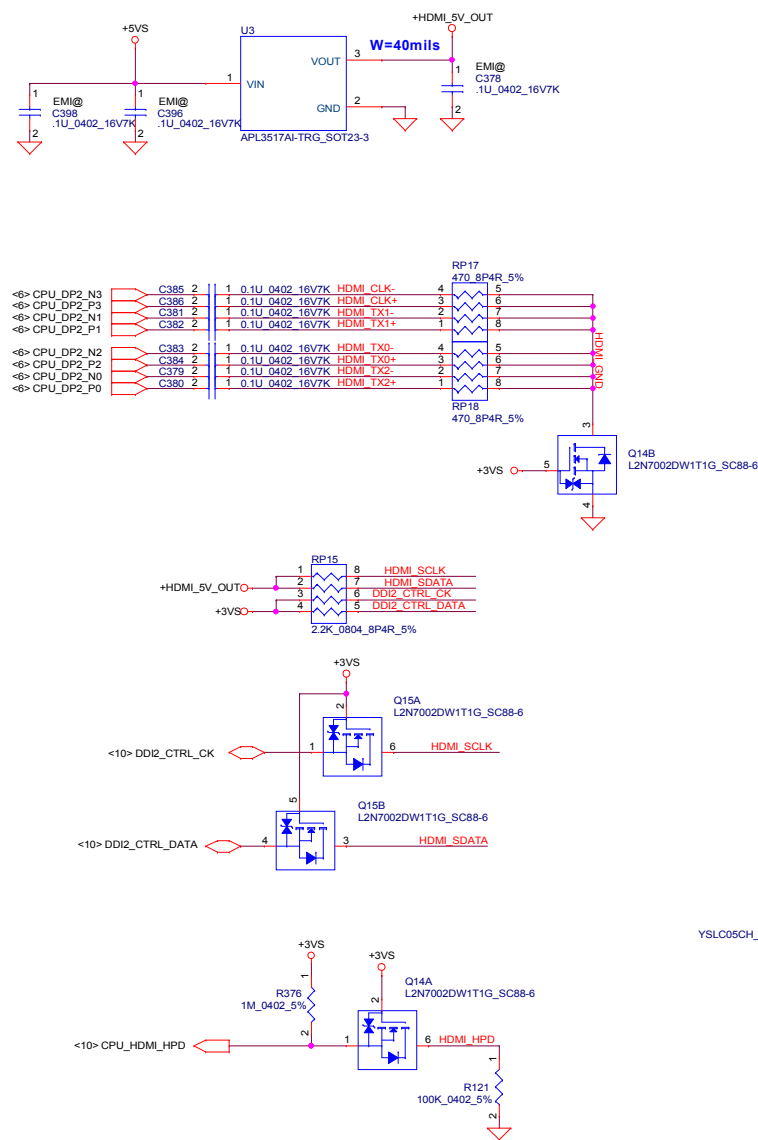


Camera



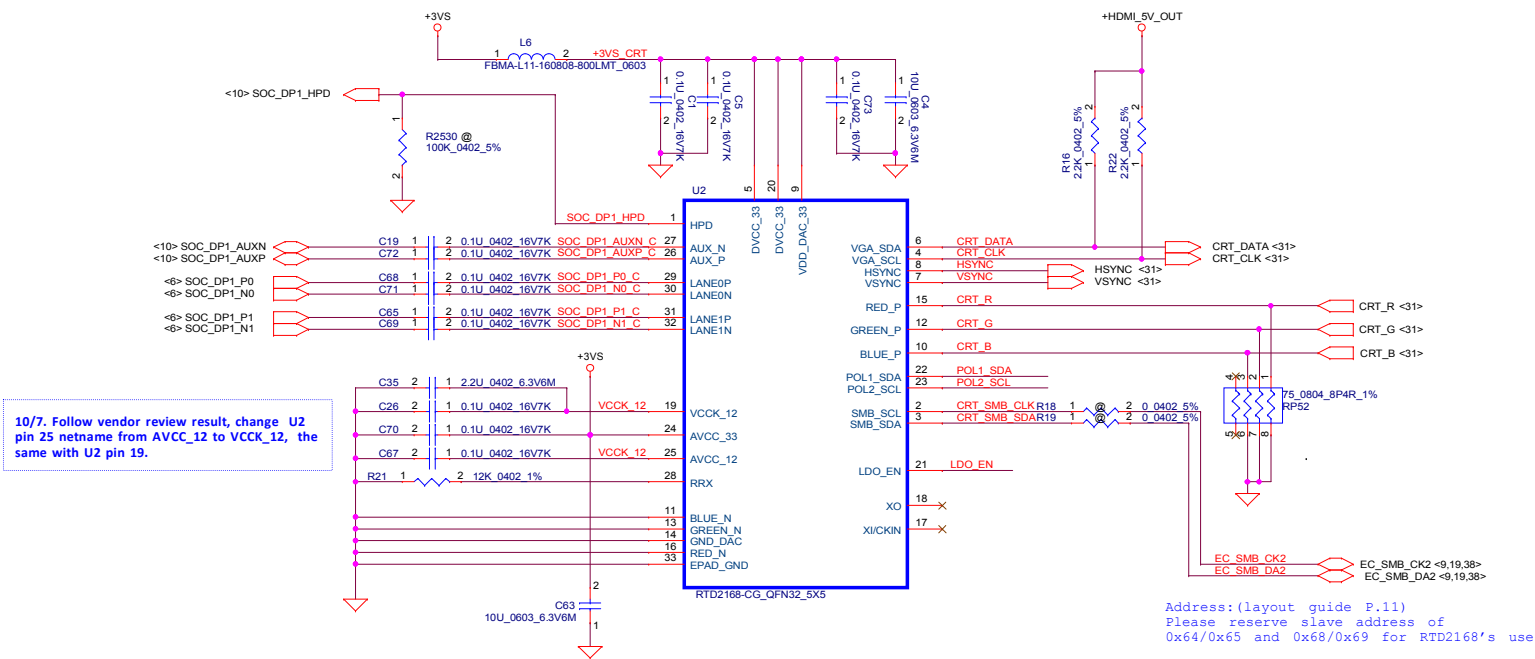
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Issued Date		2014/09/16		Deciphered Date	
				2014/05/24	
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				eDP Connector	
				Document Number	
				Customer	
				A4WB M/B LA-C341P	
				Rev	
				0.2	
				Date: Wednesday, March 18, 2015	
				Sheet 28 of 56	

HDMI conn.

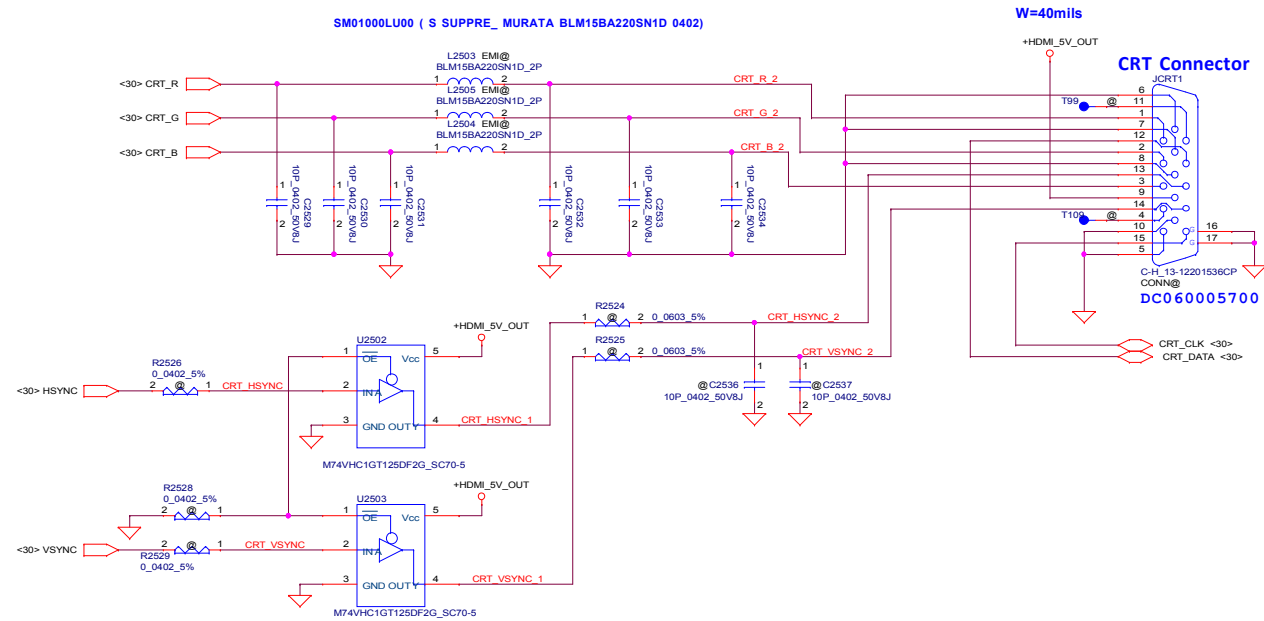


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Issued Date	2014/09/16	Deciphered Date	2014/05/24	Title
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DP to VGA Realtek RTD2168

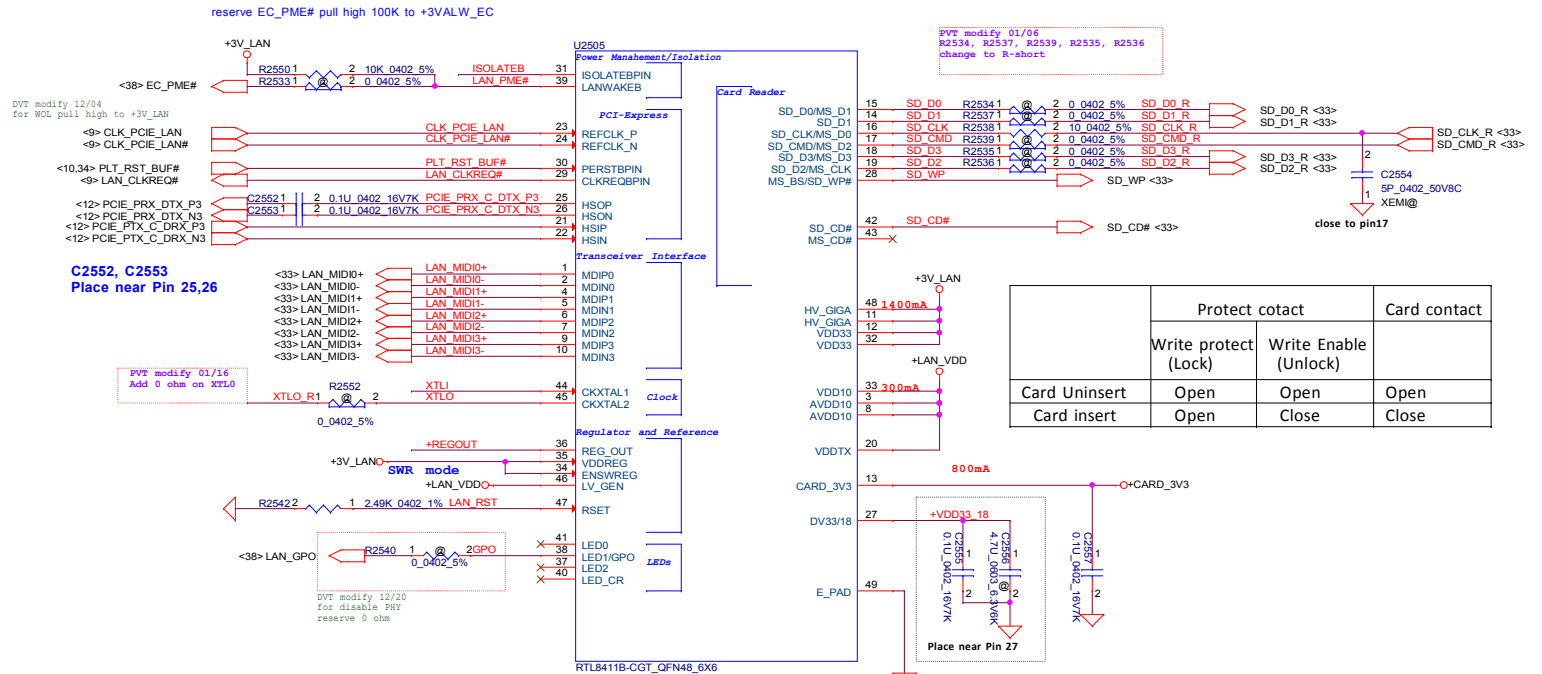
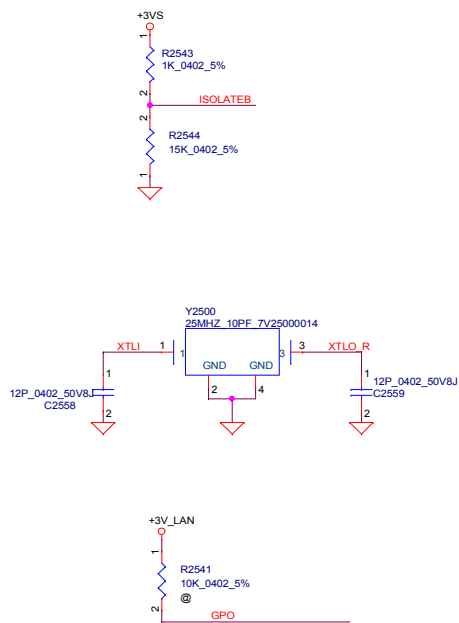
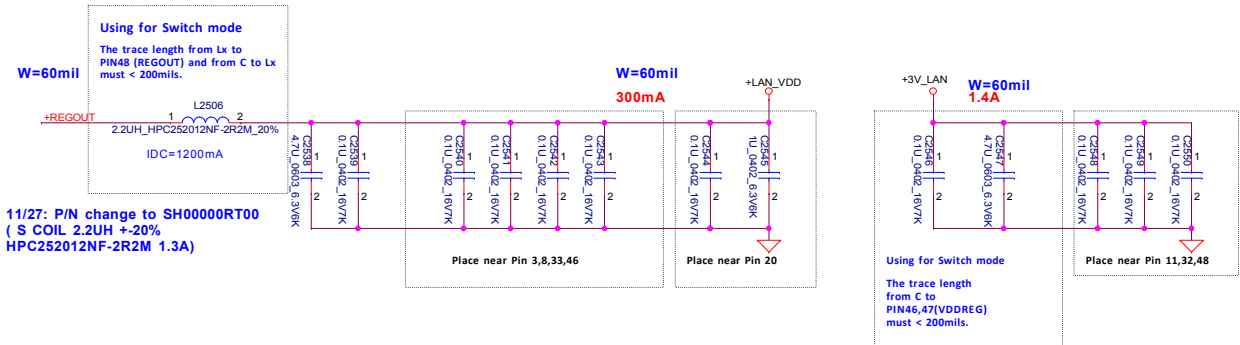
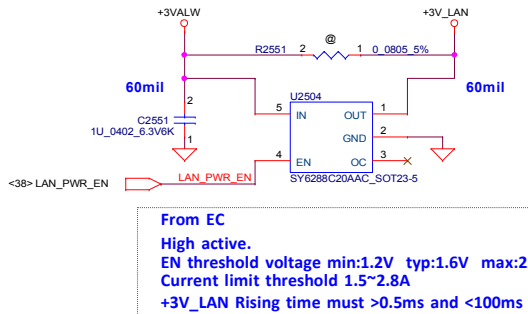


CRT conn.



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				Size	Document Number	Rev	
				A4WAB M/B LA-C341P			
				Date:	Wednesday, March 18, 2015	Sheet	31 of 56

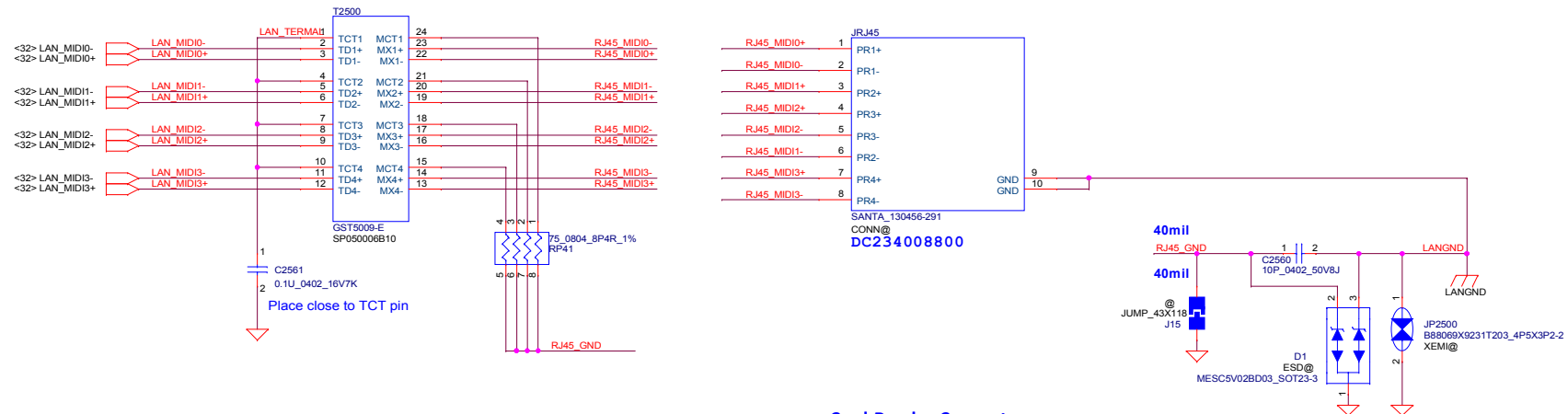
LAN-RTL8411B



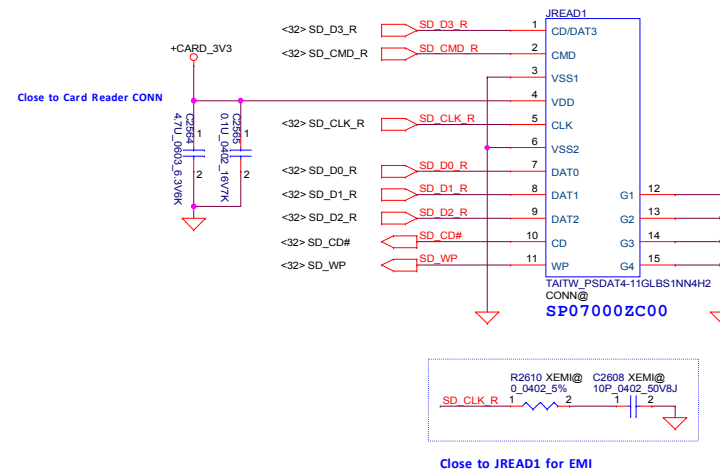
	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

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Issued Date	2014/09/16	Deciphered Date	2014/05/24	Title	LAN RTL8411-CG
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RJ45 / Card Reader conn.



Card Reader Connector

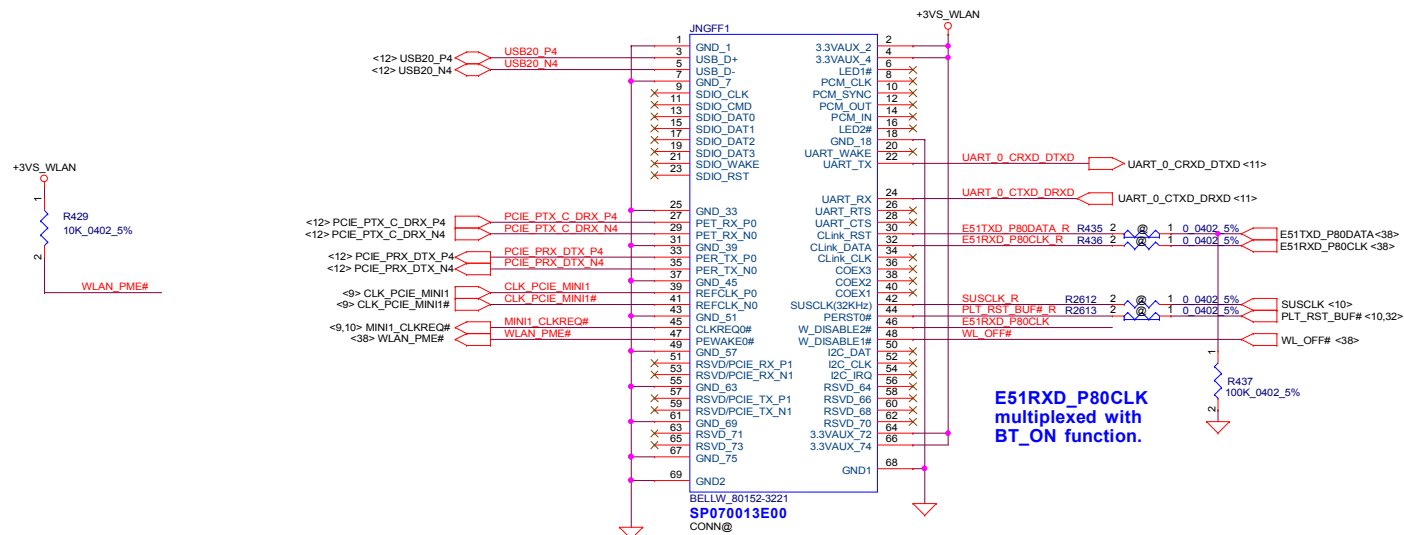


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Wireless LAN

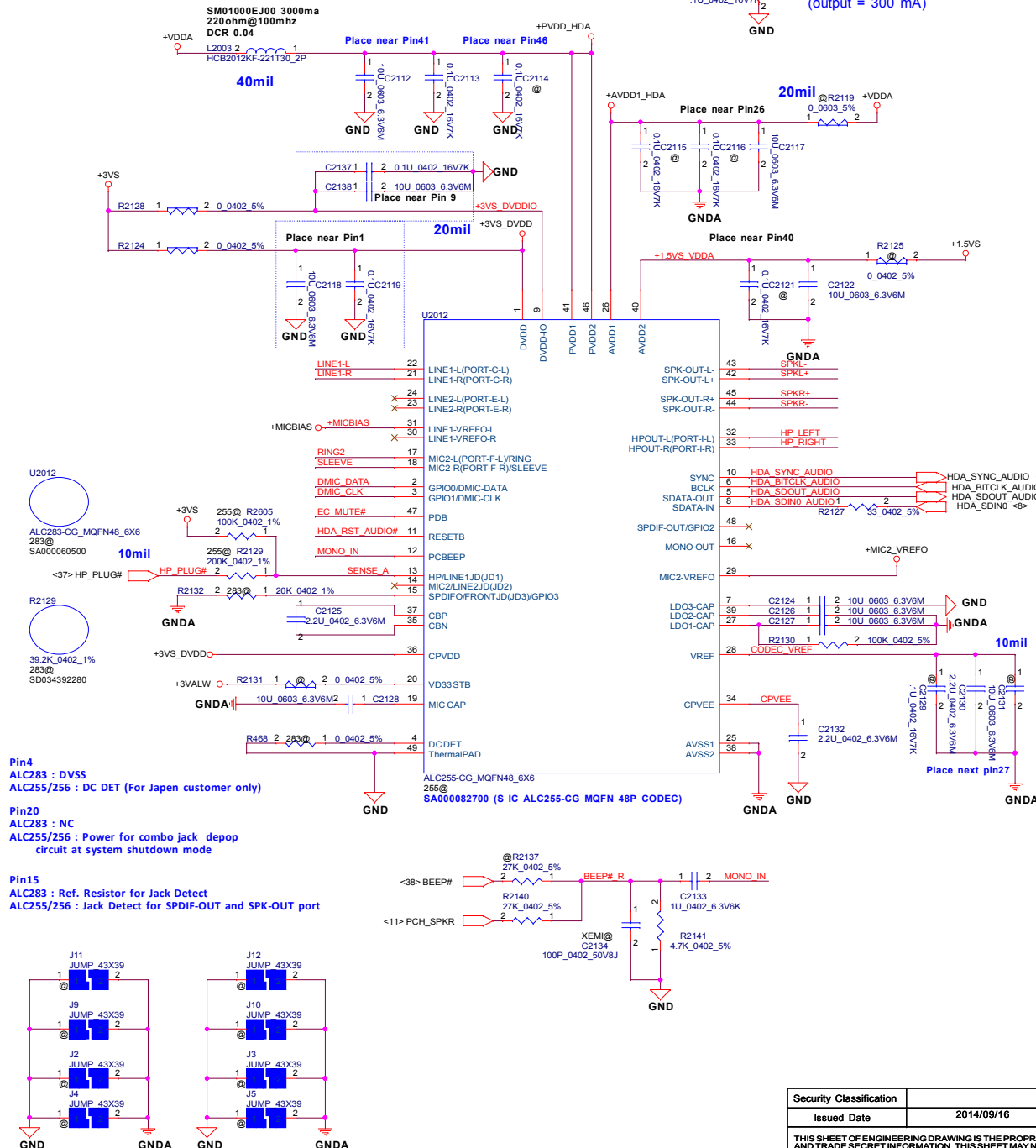


NGFF Card E key module pin define

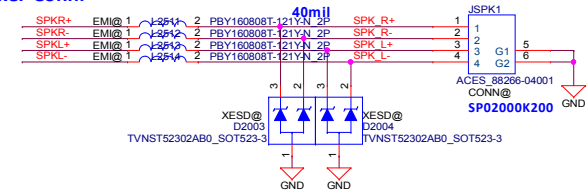


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				Date	Wednesday, March 18, 2015
				Sheet	34 of 56

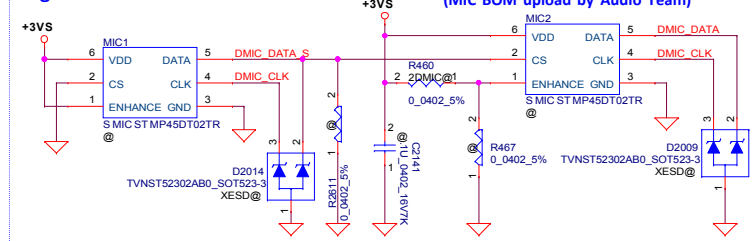
HD Audio Codec



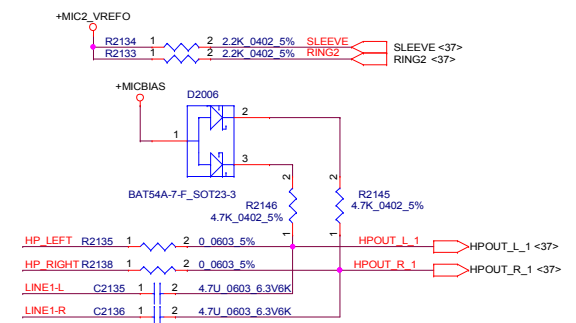
Int. Speaker Conn.



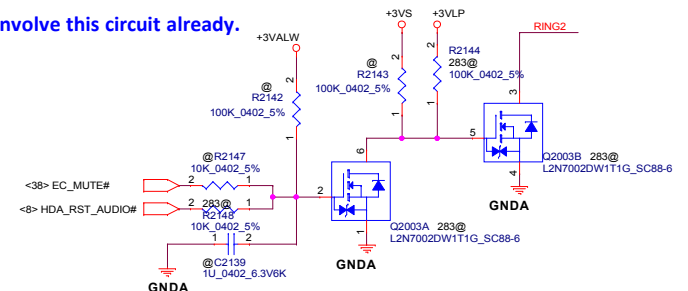
Digital Mic



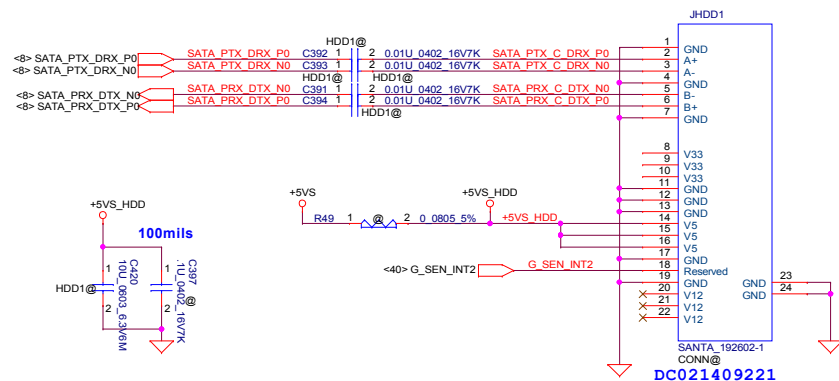
Headphone out



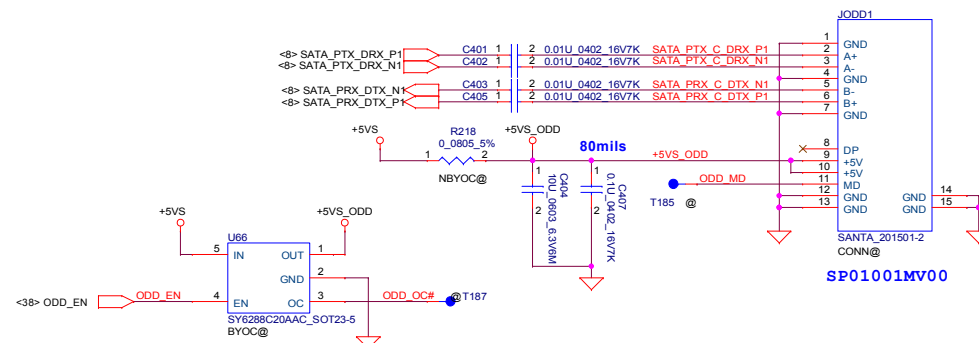
255 involve this circuit already.



SATA HDD1 Conn.



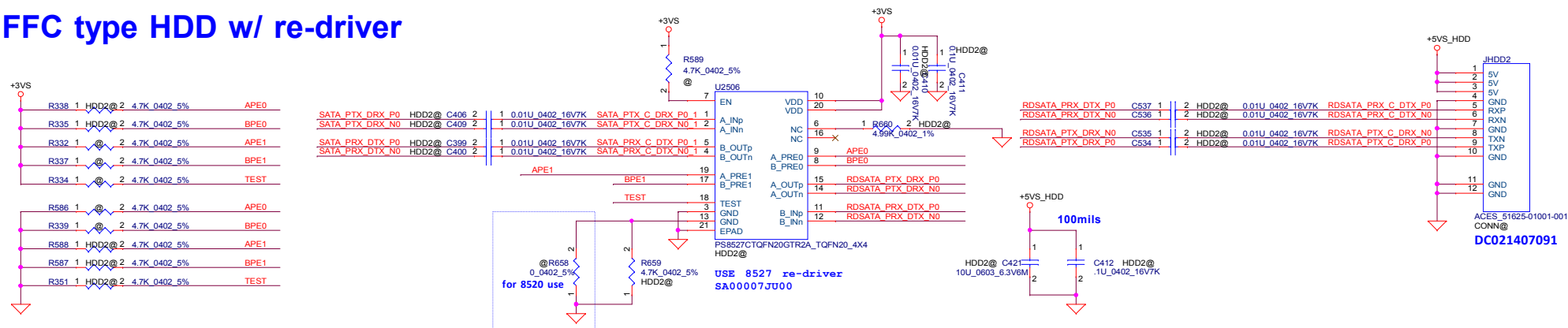
SATA ODD Conn.



FFC type HDD w/o re-driver

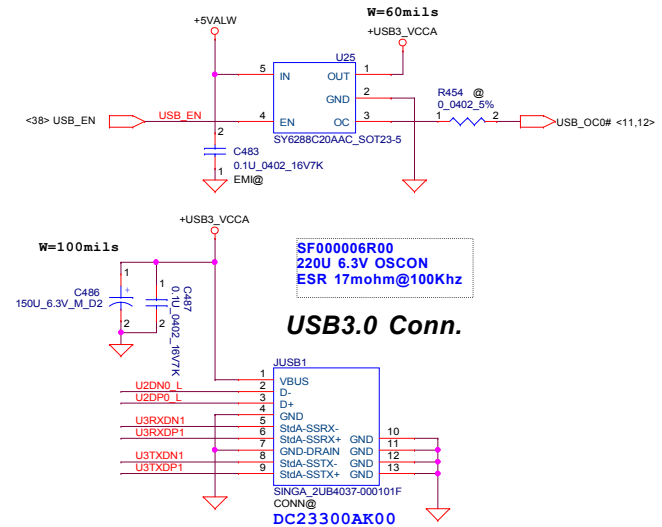
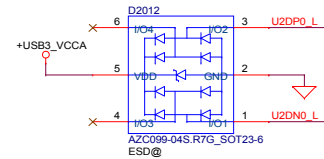
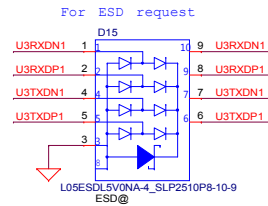
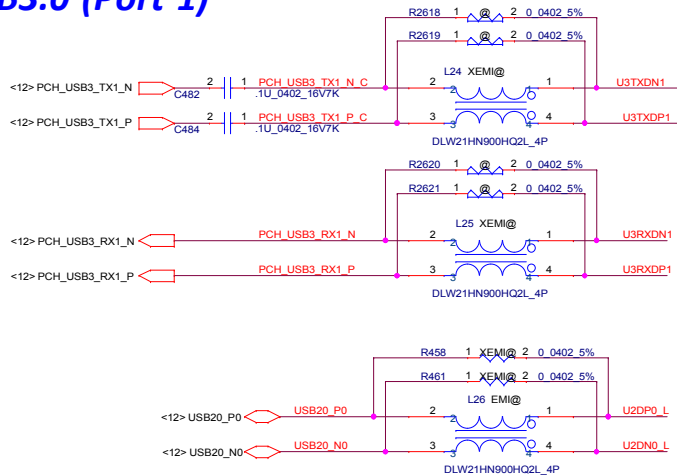


FFC type HDD w/ re-driver

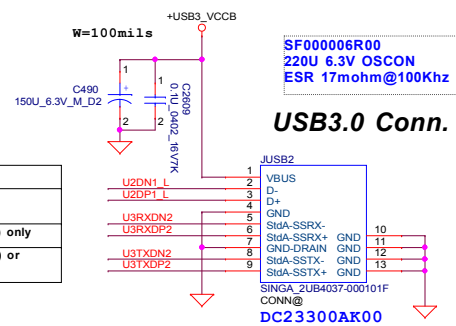
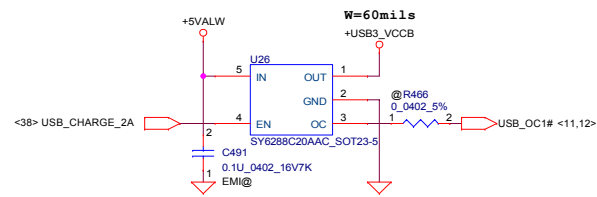
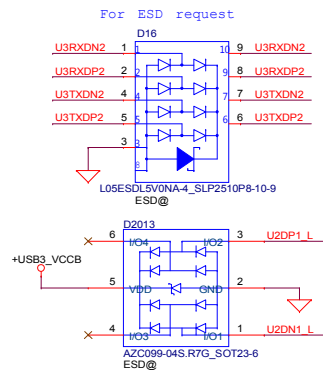
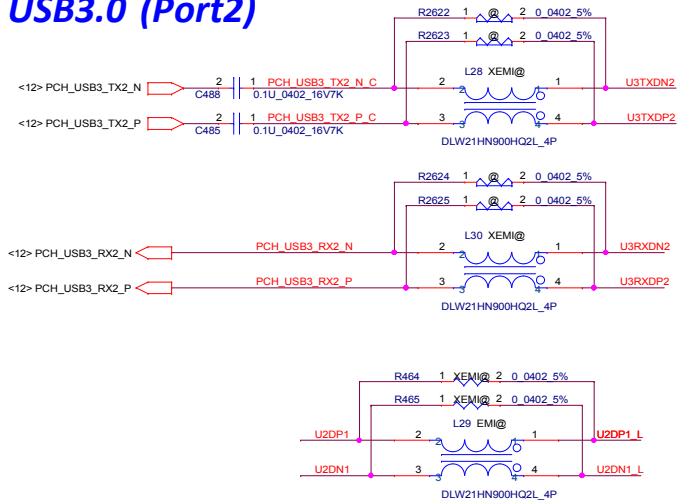


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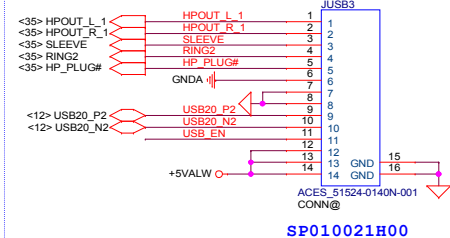
USB3.0 (Port 1)



USB3.0 (Port2)

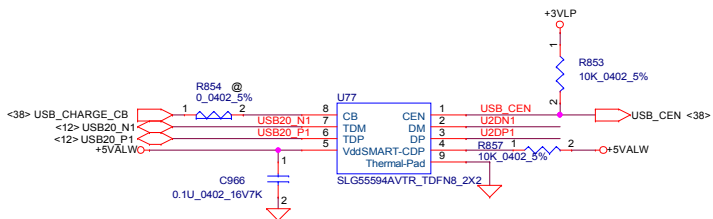


USB/B (USB 2.0 + AUDIO)
Need check Audio Pin Sequence

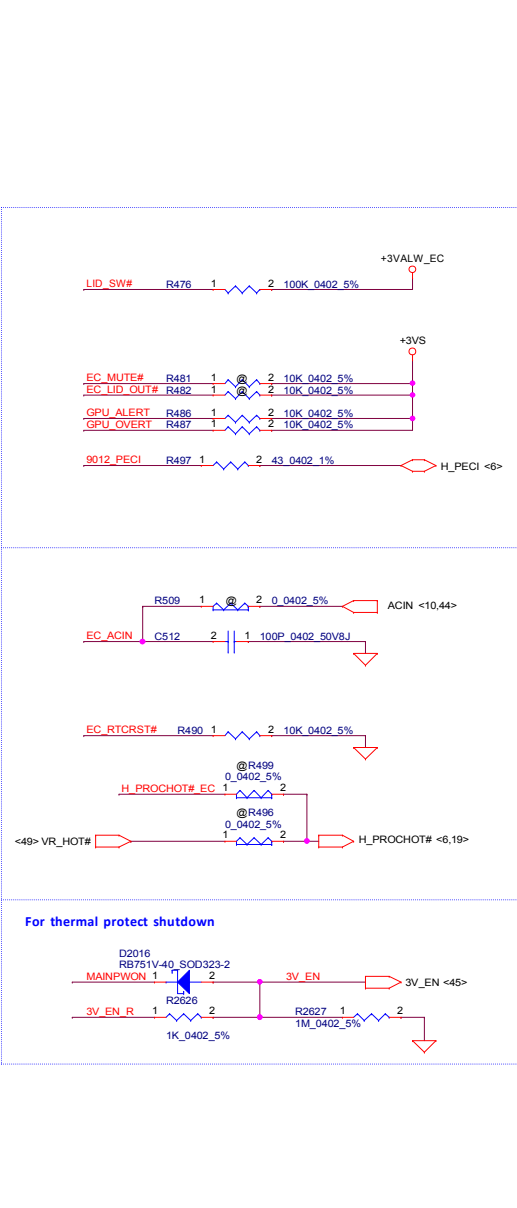


USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only

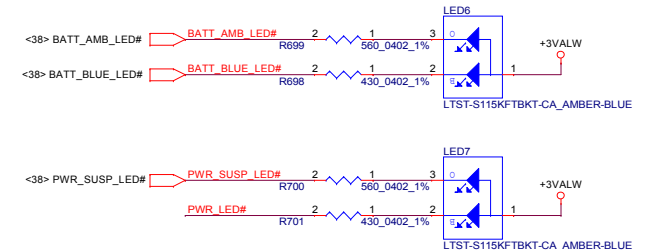
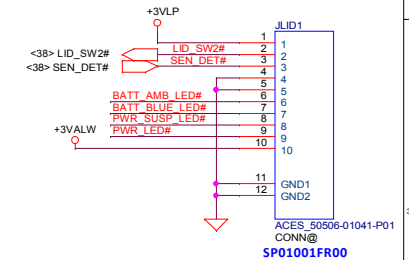


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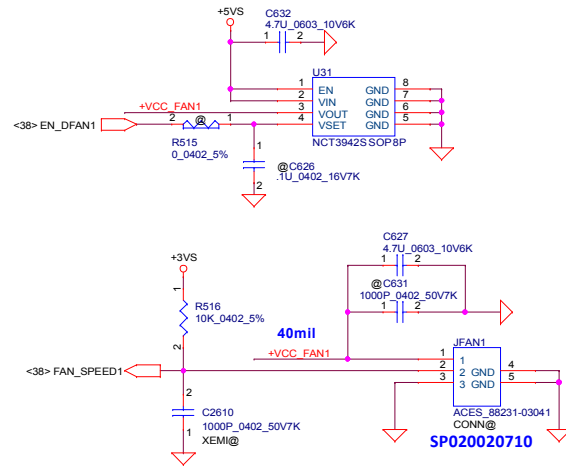
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Issued Date	2014/09/16	Deciphered Date	2014/05/24	Title	EC ENE-KB9022	
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				A4WAB M/B LA-C341P		
C		D		Date:	Wednesday, March 18, 2015	Sheet 38 of 56

KB BackLight

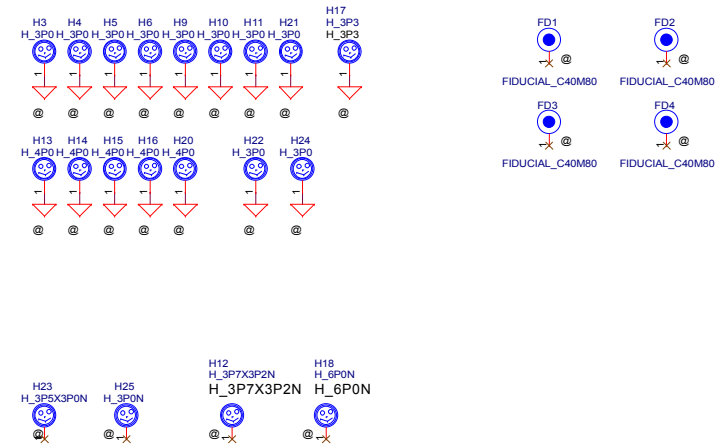


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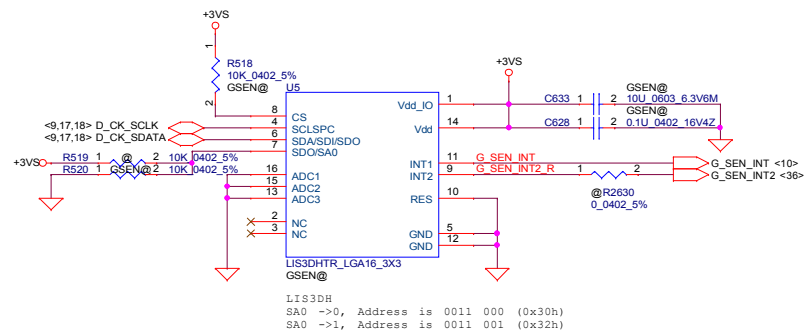
FAN1 Conn



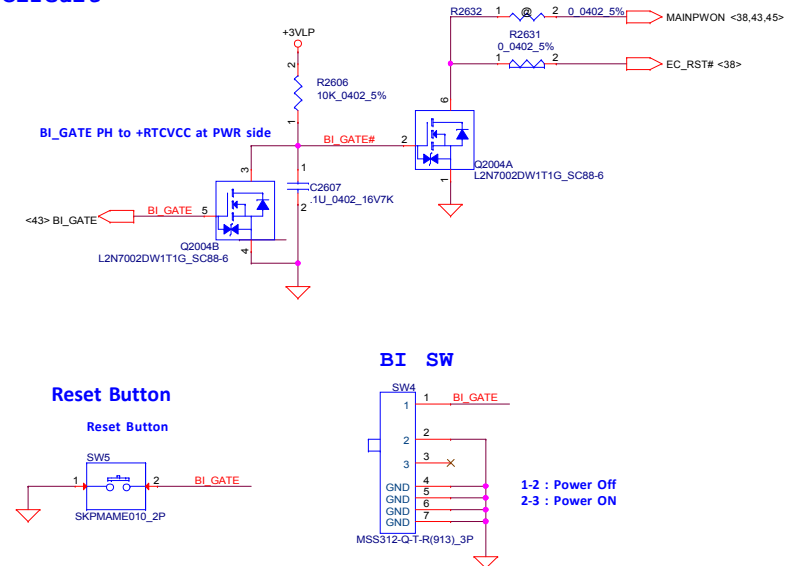
Screw Hole



G-Sensor

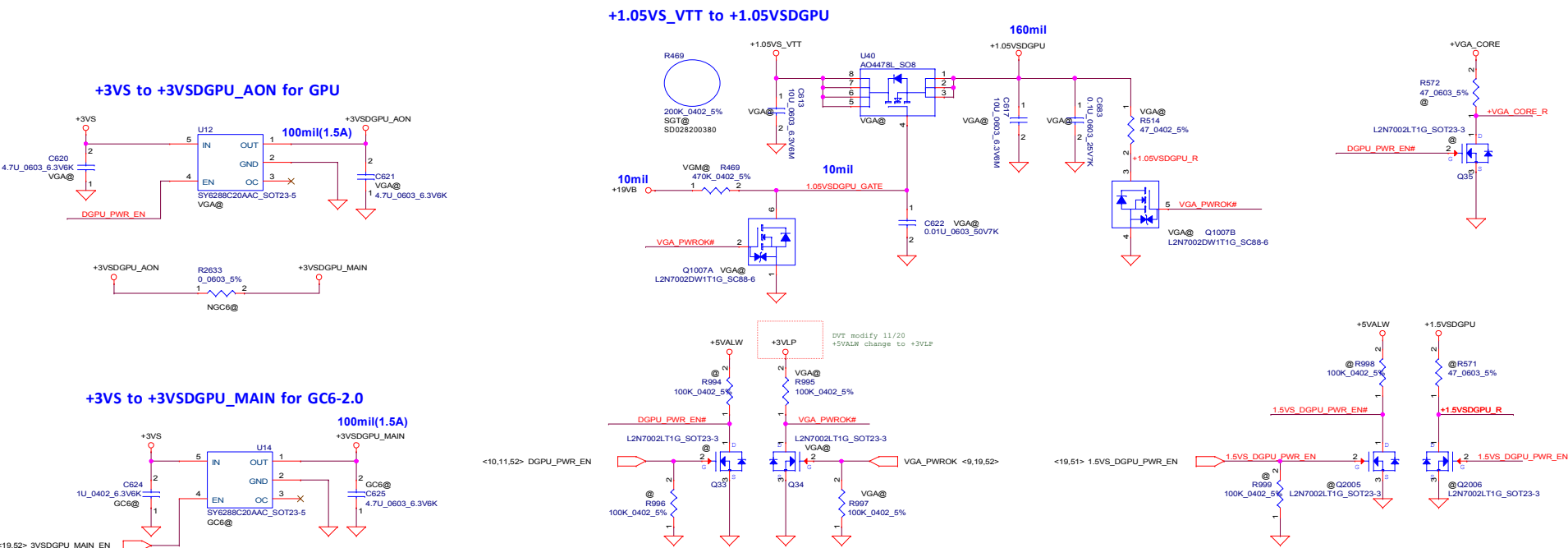
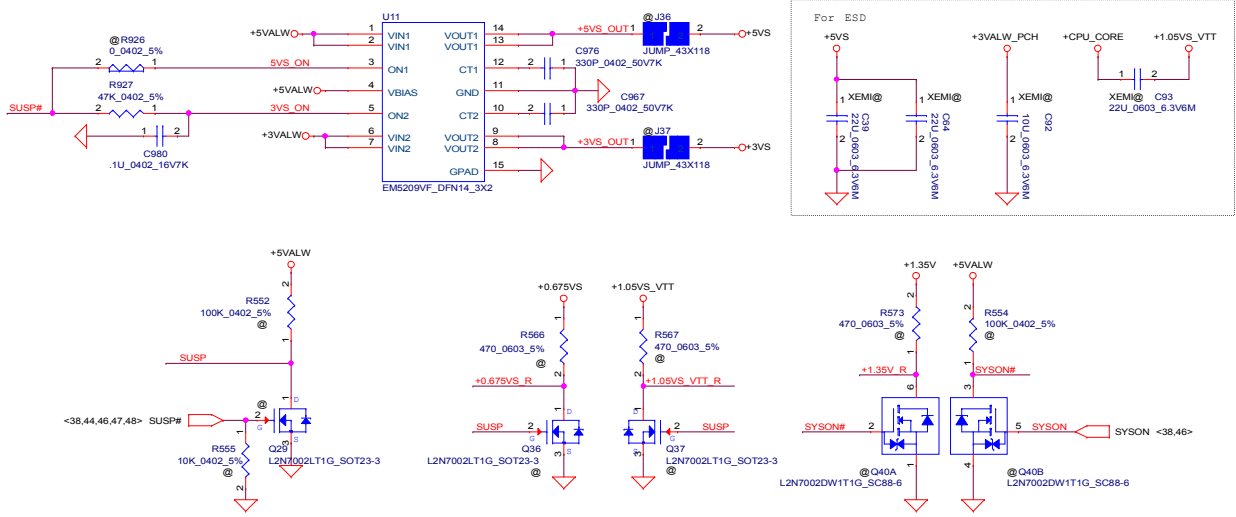


Reset Circuit



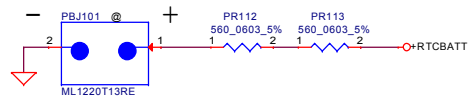
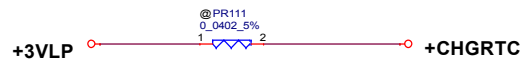
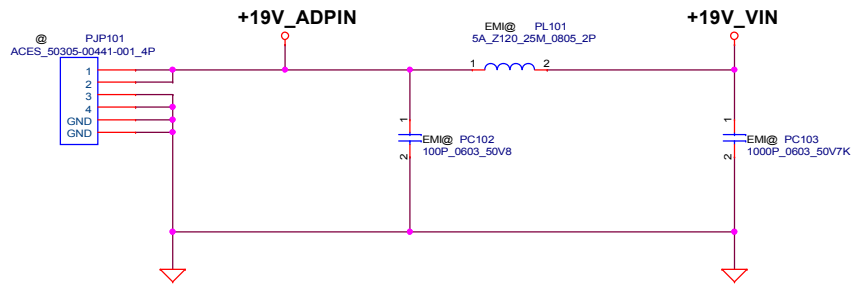
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Issued Date	2014/09/16	Deciphered Date	2014/05/24	Title	
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				Part Number A4WAB M/B LA-C341P	Rev 0.2
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DC & VGA Interface

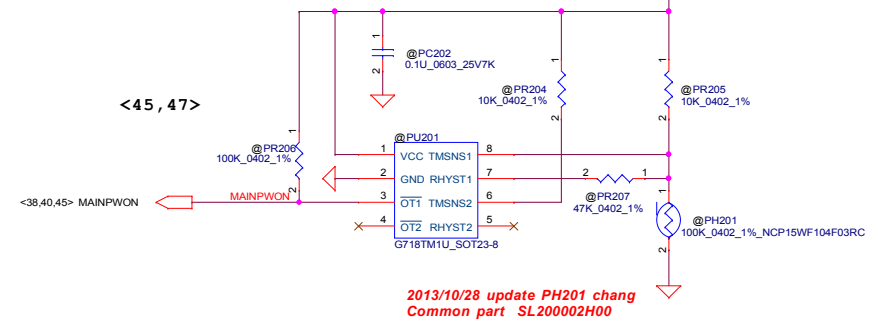
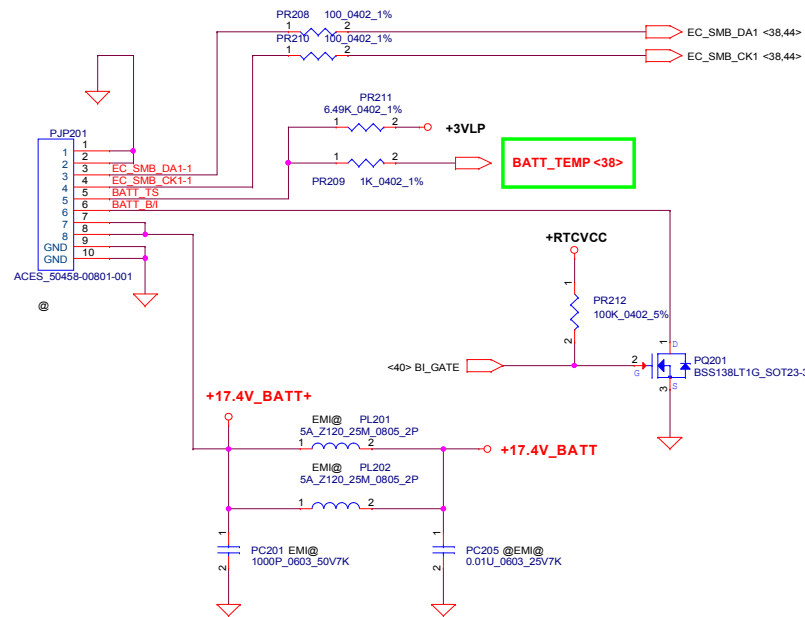


3VSDGPU_MAIN_EN From GPU

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				DC Interface			
				Size	Document Number	Rev	
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				Custom	1.0
				Date: Wednesday, March 18, 2015	Sheet 42 of 56



2013/10/28 update PH201 chang
Common part SL200002H00

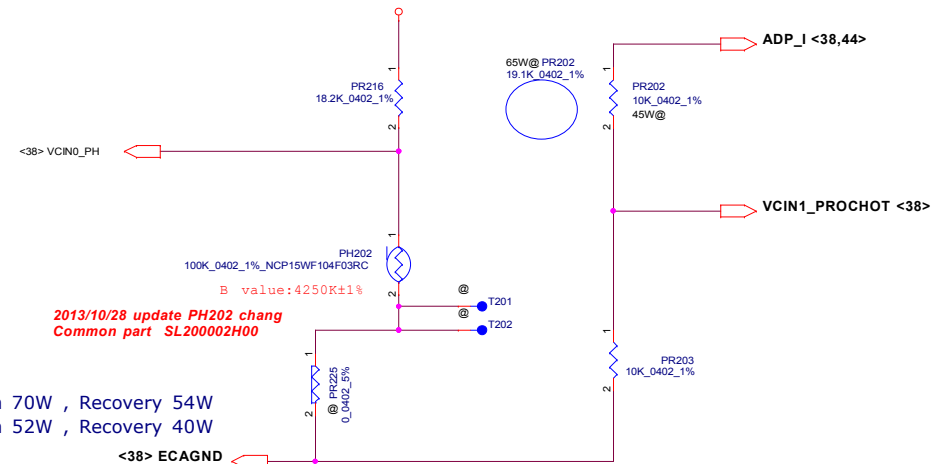
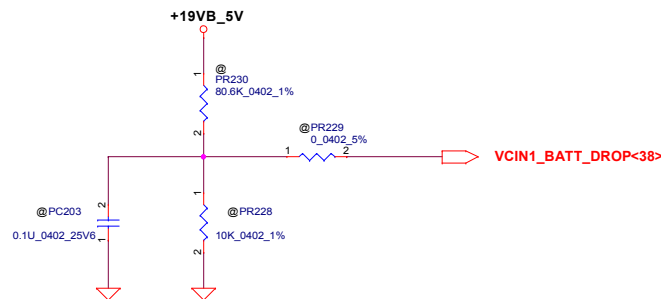
2014/09/30 update

For KB9022 sense 20mΩ	Active	Recovery
45W PR202 10K ohm SD034100280	58.5W, 0.61V	45W, 0.47V
65W PR202 19.1K ohm SD034191280	84.5W, 0.61V	65W, 0.47V

PH202 under CPU bottom side :
CPU thermal protection at 90 degree C (shutdown)
Recovery at 56 degree C +EC_VCCA

2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

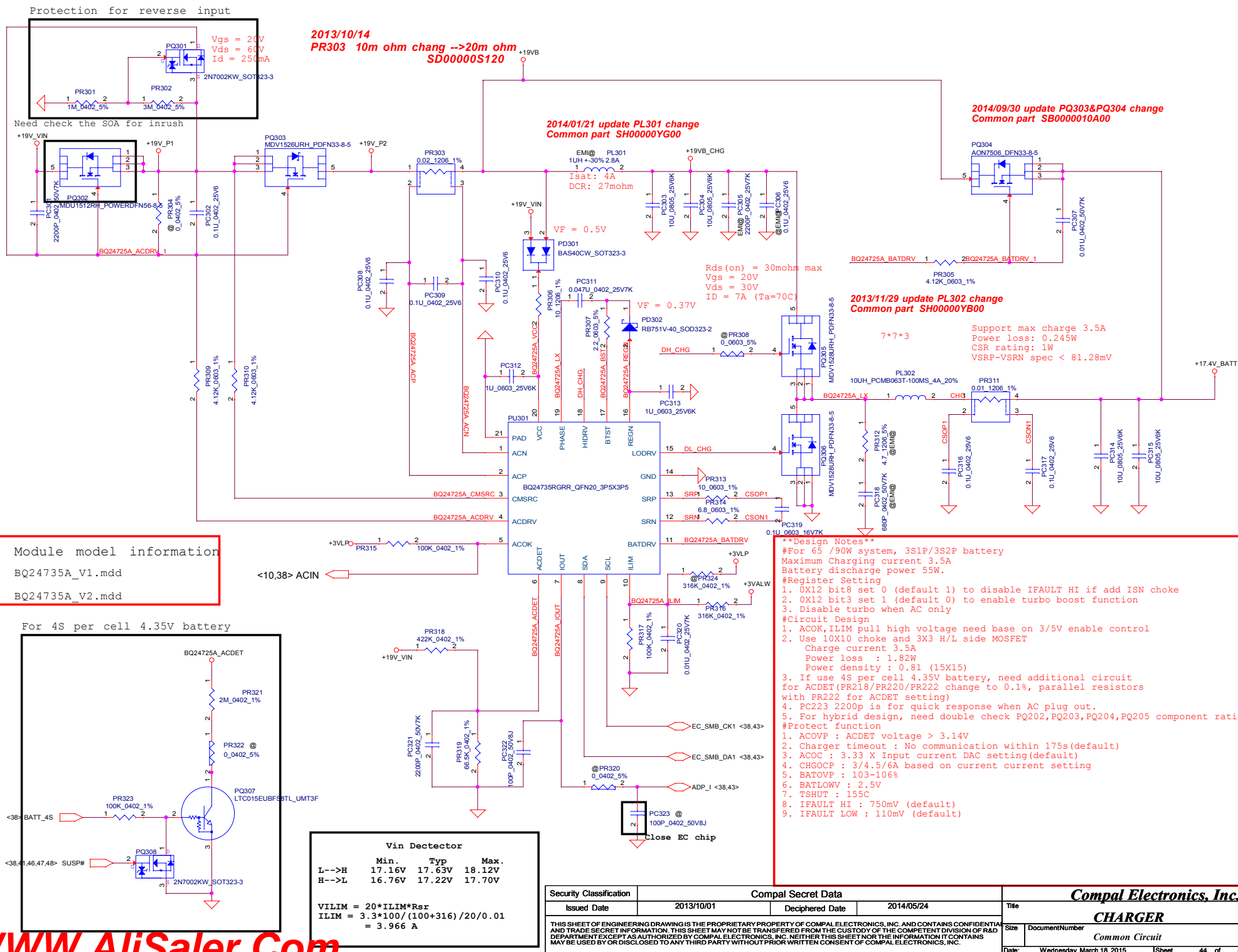
Battery is 3-cell design.
B+=9V



2013/10/28 update PH202 chang
Common part SL200002H00

For 65W adapter==>action 70W , Recovery 54W
For 40W adapter==>action 52W , Recovery 40W

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				Document Number
				Rev
				1.0
				Date: Wednesday, March 18, 2015
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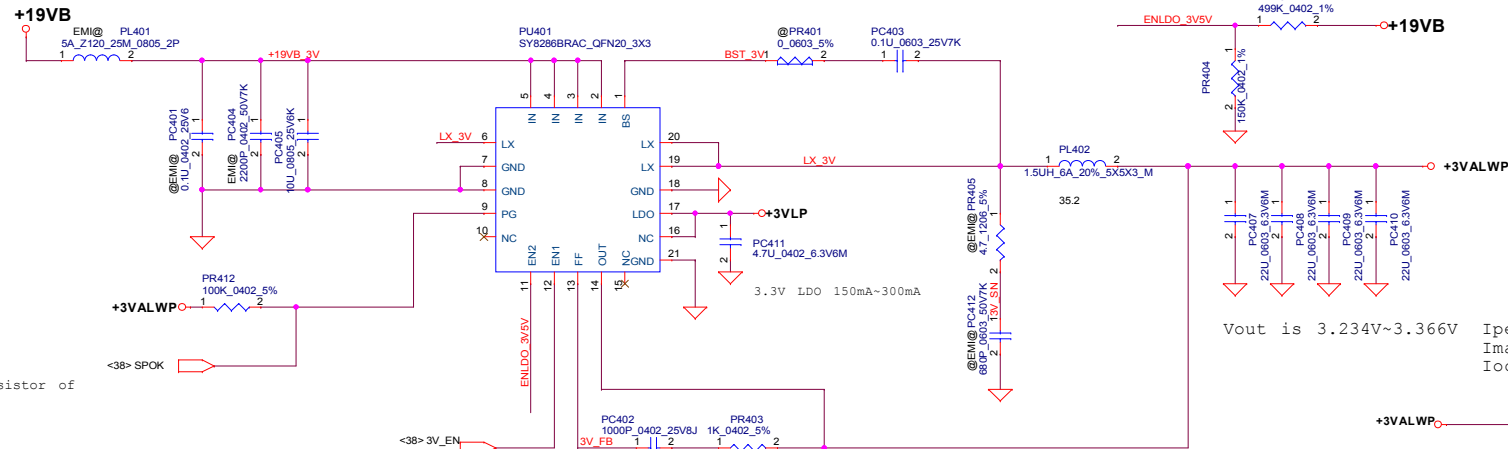
Module model information

SY8208B_V2.mdd

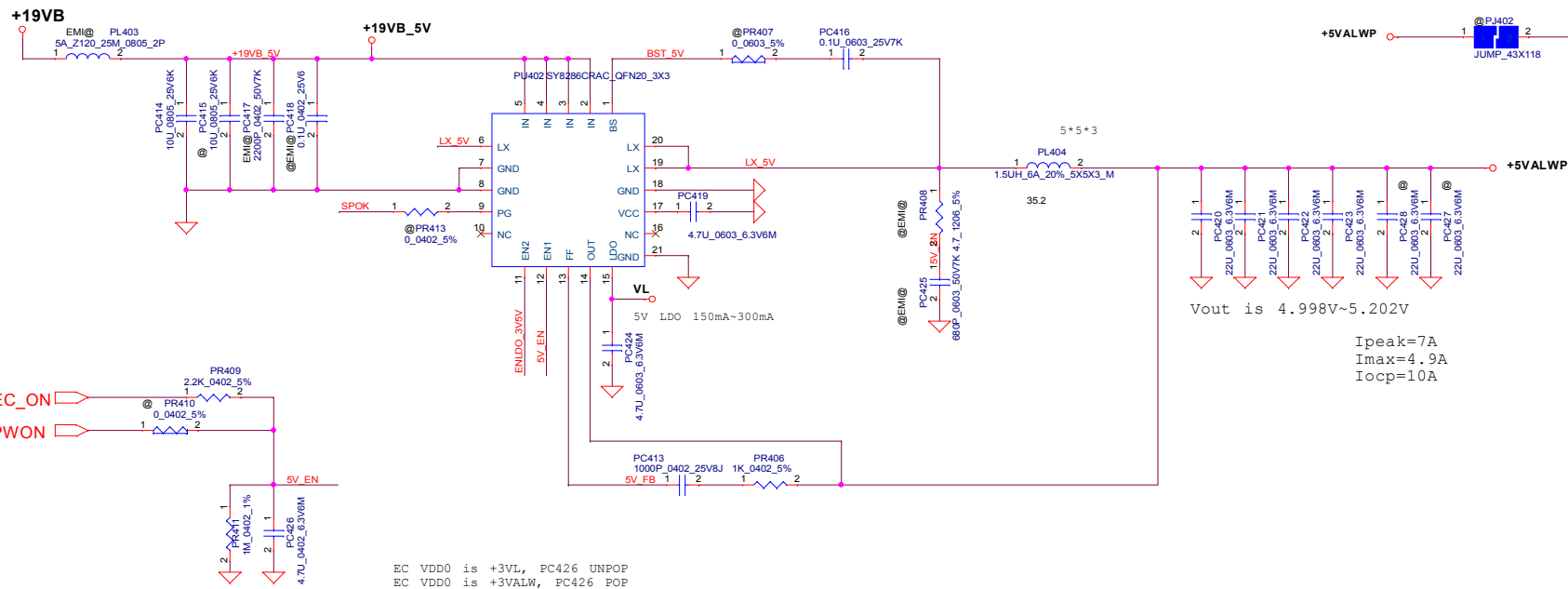
SY8208C_V2.mdd

EN1 and EN2 don't floating

Check pull up resistor of
SPOK at HW side



Vout is 3.234V~3.366V Ipeak=7A
Imax=4.9A Iocp=10A



Vout is 4.998V~5.202V Ipeak=7A
Imax=4.9A Iocp=10A

EC VDD0 is +3VL, PC426 UNPOP
EC VDD0 is +3VALW, PC426 POP

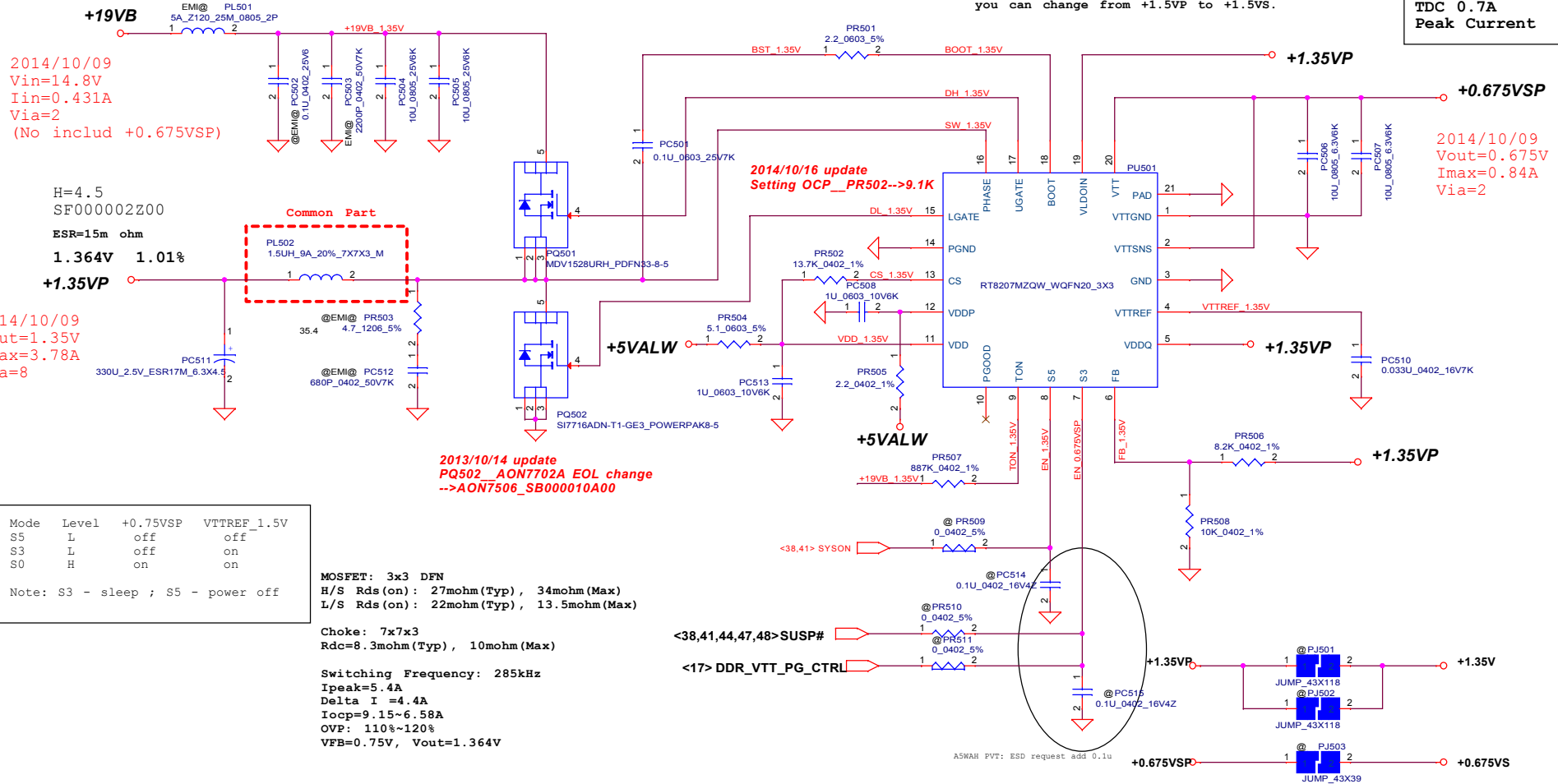
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Issued Date	2013/10/01	Deciphered Date	2014/05/24	Title +3VALW/+5VALW	
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Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



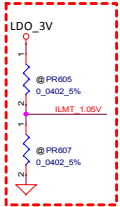
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				Custom
				Date: Wednesday, March 18, 2015
				Sheet 46 of 56
				Rev 1.0

Compal Electronics, Inc.

+1.35VP/+0.675VSP

```
Module model information
SY8208D_v1.mdd
```

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

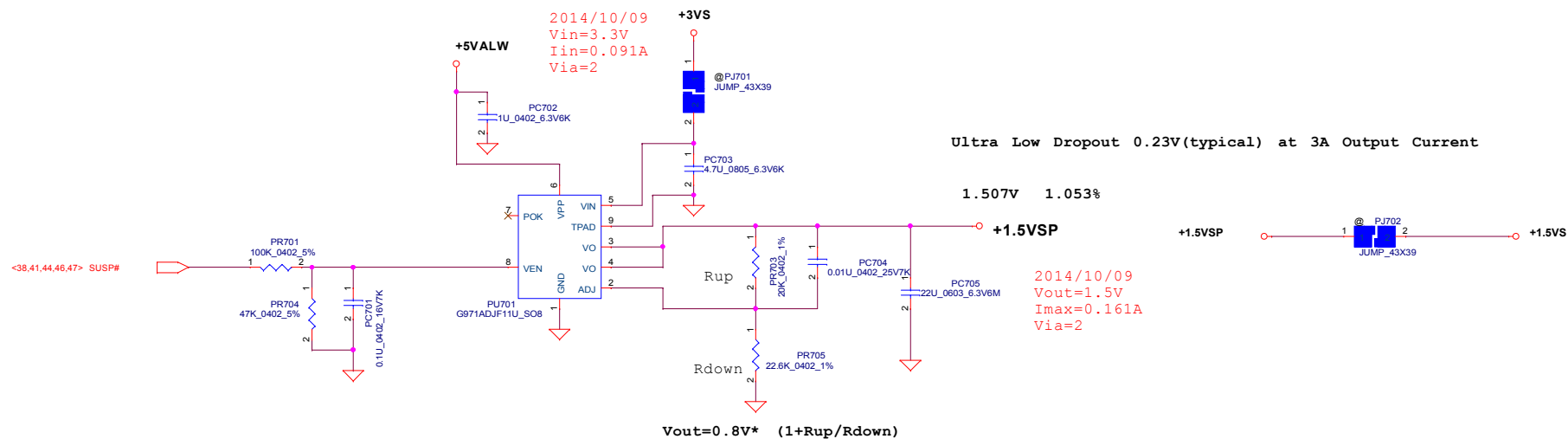


PR606 part count reduce

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Module model information
SY8208D_V1.mdd

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Module model information:
ISL95813 (for 15W & 28W CPU)

Base on BDW PDDG Rev_0_73

Location	15W	28W	Note
	TDC 14A	TDC 19A	
	MAX 32A	MAX 40A	
	OCF 38.4A	OCF 48A	
	Loadline=-2.0mv/A	Loadline=-2.0mv/A	
PR820	392 Ohm	499Ohm	OCF
PR816	1.27kOhm	1.58kOhm	Droop
PC816	0.033uF	0.022uF	RC Match
PR804	90.9kOhm	113kOhm	PROG1
PR807	93.1kOhm	95.3kOhm	IMON
PC811	0.1uF (0402)	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

-->20130828
Choke: 0.15uH (Size:7*7*4)
SH00000U300
Rdc=0.66mohm +-7%
Heat Rating Current=36A
Saturation Current=45A

Note:
VR_SVID_ALRT# Pull high on HW side

Note:
PR804=113K
=>lcc(max)=40A
fsw=700KHz

Note:
PR812=124K
=>Slew rate=53mV/us
Vboot = 1.7V

Over temperature protection:
OTP Setting: 100C active
Pin5 (NTC) voltage <0.88V, Protect
Pin5 (NTC) voltage >0.92V, recovery

2013/10/28 update PH802 chang
Common part SL200002E00

2014/01/21 update PL802 change
Common part SH000011H00

2013/10/28 update PH801 chang
Common part SL200002G00

PL803 EM@
5A_Z120_25M_0805_2P
PL801 EM@
5A_Z120_25M_0805_2P
+19VB
Height 8 mm
100u_SF000000I80
2014/10/09
Vin=14.8V
Iin=3.193A
Height 6 mm
68u_SF000000W00
Via=8

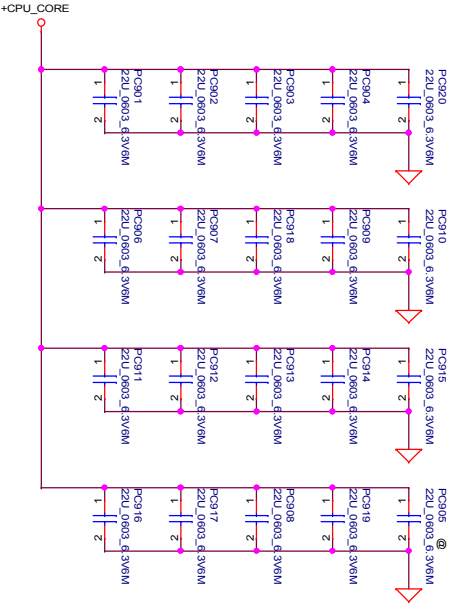
TDC 19A
MAX 40A
OCF 48A
Loadline=-2.0mv/A

2014/10/09
Vout=1.35V
Imax=28A
Via=56

Local sense put on HW site

123	
CPU CORE/GFX CORE	
Size	Document Number
A4WAB M/B LA-C341P	
Date: Wednesday, March 18, 2015	Sheet 49 of 56

PWR Rule
需確認最新SPEC.
Modify 8/6.

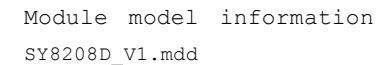


30 X 22uF 0805
2012/10/23
check the output cap Qty!!!
2012/10/24
23 pcs 22uF and reserve 7 pcs
2013/01/14
22uF*17 unpop:22uF*3

20130828
15W: 22uF*14
28W: 22uF*16

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				CPU CORE CAP				
				Size	Document Number		Rev	
				Custom			1.0	
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The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high



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Module model information:
RT8813A_V1A for IC module
RT8813A_V1B for SW module

$V_{boot} = V_{ref} \cdot R_{ref2} / (R_{ref1} + R_{ref2} + R_{boot})$
 $R_t = R_{refadj} \parallel (R_{boot} + R_{ref2})$
 $V_{min} = V_{ref} \cdot [R_{ref2} / (R_{ref2} + R_{boot})] \cdot [R_t / (R_{ref1} + R_t)]$
 $V_{max} = V_{ref} \cdot R_{ref2} / [(R_{ref1} / R_{refadj}) + R_{boot} + R_{ref2}]$
 $V_{out} = V_{min} + N \cdot V_{step}$
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

PWM-VID Spec and component Values

PWM-VID Spec		Config B	Config C	Config D
Vmin		0.6V	0.65V	0.9V
Vmax		1.2V	1.15V	1.15V
Vboot		0.9V	0.9V	1.028V
Voltage step		6.25mV	25mV	12.5mV
N of Voltage level		96	20	20
Rrefadj	PR1209	20K	39K	27K
Rref1	PR1208	20K	30K	7.5K
Rboot	PR1211	2K	3K	0
Rref2=PR1210	PR1210	18K	24K	6.2K
+PR1224	PR1224	0	3K	1.74K
C	PC1210	2.7nf	1.8nf	5.6nf

N15S-GT N15V-GL N15V-GM
N16S-GT
N16V-GM

PSI :
1 phase with DEM 0V to 0.8V
1 phase with CCM 1.2V to 1.8V
2 phase with CCM 2.4V to 5.5V

EN High Threshold = 1.6V

Current Limit threshold setting
 $R_{ocset} = (I_{valley} \cdot R_{ds(on)} + 40 \text{ mV}) / 10 \mu\text{A}$

$I_{ripple} = (19-0.9) \cdot 0.9 / (304.89 \text{ Khz} \cdot 0.36 \mu\text{H}) = 7.811 \text{ A}$

$OCP = 54 \text{ A} / 2 = 27 \text{ A}$ per phase
 $I_{valley} = 27 \text{ A} \cdot 7.811 \text{ A} / 2 = 23.1 \text{ A}$

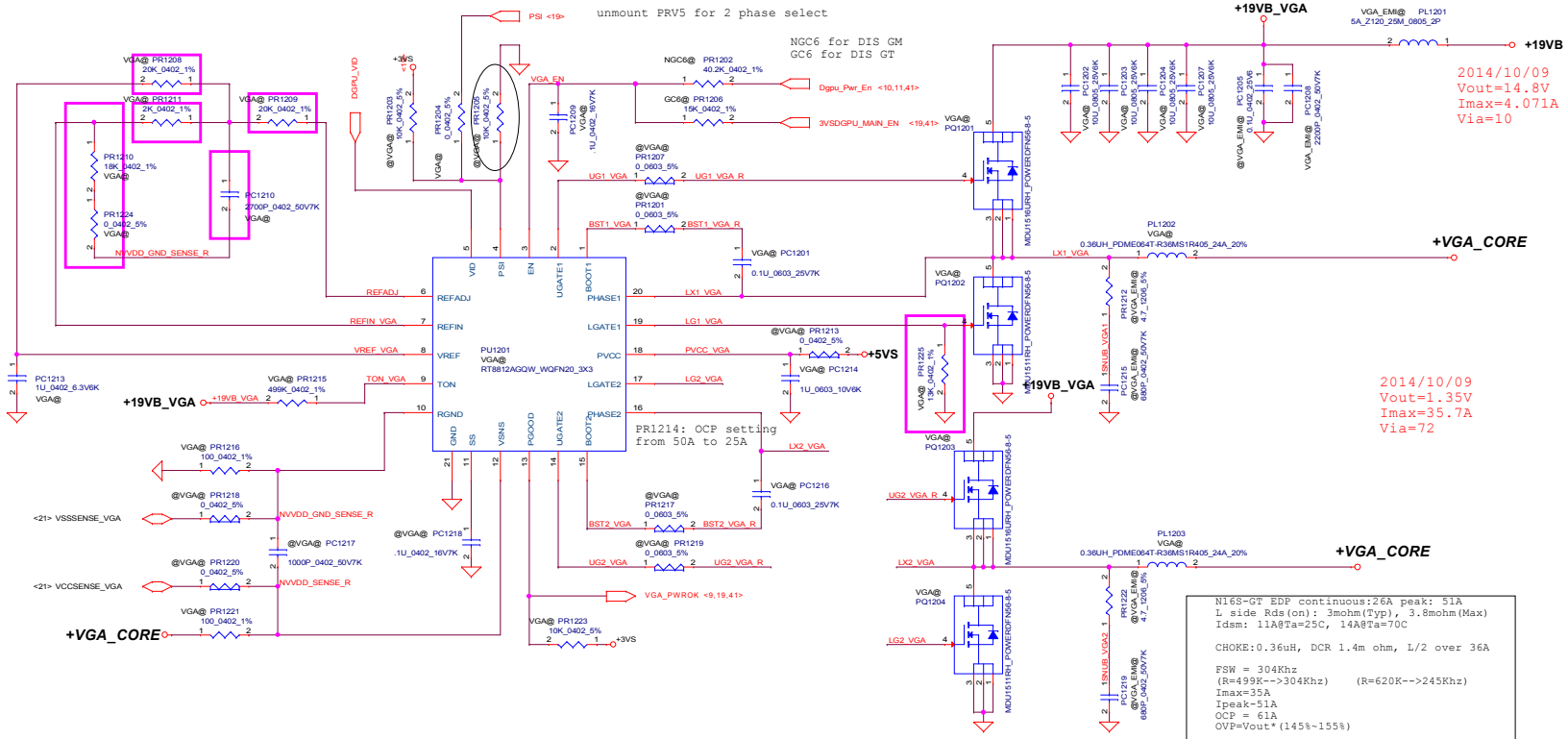
H-side MOS:AON6552 L-side MOS:AON6554
 $R_{ds(on)}$: 5.6mohm@Vgs=10V 3.2mohm@Vgs=10V
6.7mohm@Vgs=4.5V 3~3.8mohm@Vgs=4.5V
 I_d : 20A@Ta=25 degC I_d : 85A@Ta=25 degC

Choke: 0.22uH (Size: 7*7*4)
 $R_{dc} = 0.97 \text{ mohm} + 5\%$
Heat Rating Current=34A
Saturation Current=25A

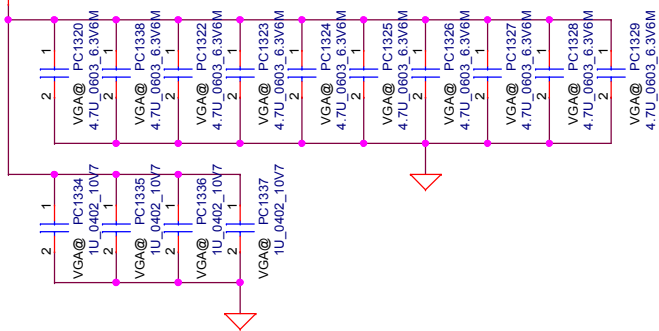
$C = 3 \cdot 330 \mu\text{F} \cdot (9 \text{ mohm}) = 990 \mu\text{F}$
 $V_{ripple} = I_{ripple} \cdot ESR(\text{min}) = 7.811 \text{ A} \cdot 3 \text{ mohm} = 23.4 \text{ mV}$

Different VGA Chip (different EDP-Peak Current) need select different solution

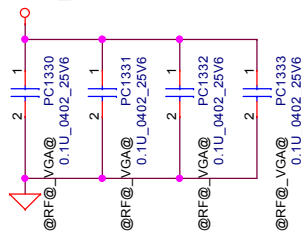
VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT	N15S-GT	N15V-GM
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config C
Rated TDP Power at Tj=102C	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W	18W	18.16W
Boosted GPU Total at Tj=102C	25W	32W	25W	20W	23W	N/A	30W	40W	25W	24.72W
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A	31A	29.2A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A	60A	75A	60A	44.3A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A		
OCP Setting Current	42A	66A	54A	42A	42A	48A	72A	90A	72A	54A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K	13K	10.2K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L	2phase 1H1L	2phase 1H1L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)		
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL	GT@	GM@



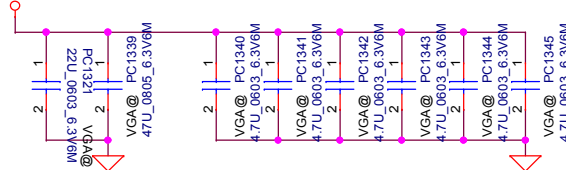
+VGA_CORE Under GPU Core GB4-128 package



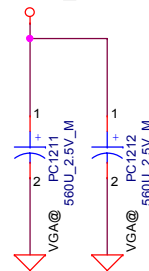
+VGA_CORE



+VGA_CORE Near GPU Core



+VGA_CORE



N15x 2013/12/10
Under
4.7uF_0603_10pcs
1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0603_1pcs (2PCS unpop)
4.7uF_0805_5pcs

N15x2013/10/17
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0603_9pcs (2PCS unpop)
4.7uF_0805_5pcs

N15x2013/10/07
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0805_9pcs (2PCS unpop)
4.7uF_0805_5pcs

N15x2013/10/02
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0805_14pcs
4.7uF_0805_5pcs

N14x
Under
4.7uF_0603_10pcs
0.1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0805_1pcs
4.7uF_0805_5pcs

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								Size	Document Number						Rev	
								Custom							1.0	
								Date:	Wednesday, March 18, 2015				Sheet	53	of	56

Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	Design Update	BOM Stucture Identical	P.51	Add GT GM2G for PR1005	20141120	DVT
2	Design Update	IC will Stop Production	P.48	Change the PU701 from APL5930KAI to G971ADJF11U	20141120	DVT
3	Design Update	Nvidia N16S-GT and N16V-GM Open VReg Configuration both use B	P.52	PR1208:20kOhm, PR120920kOhm, PR1210:18kOhm PR1211:2kOhm, PR1224:0Ohm, PC1210:2700pF PR1225:13kOhm	20141120	DVT
4	Design Update	CPU Load Line Request	P.49 P.50	Change the PR817 from 4.99MOhm to 20MOhm. Change the PR807 from 121kOhm to 93.1kOhm. Change the PR813 from 1.91kOhm to 3.65kOhm. Change the PC917 PC908 and PC919 from @ to 22uF.	20141128	DVT
5	Design Update	Solution Change	P.45 P.47 P.51	Change the PU401 from SYX198BQNC to SY8286BRAC Change the PU402 from SYX198CQNC to SY8286CRAC Change the PU601 from SYX198DQNC to SY8288RAC Change the PU1001 from SYX198DQNC to SY8288RAC	20141128	DVT
6	Design Update	RC Value for GPU Sequence Fine Tune GC6 Function	P.51 P.52	GM: PR1002:15kOhm, PC1002:0.1uF. GT: PR1002:4.7kOhm, PC1002:0.1uF. GM(No Support GC6, Use DGPU_PWR_EN) PR1202:40.2kOhm, PC1209:0.1uF. GT(Support GC6, Use 3VSDGPU_MAIN_EN) PR1206:20kOhm, PC1209:0.1uF.	20141128	DVT
7	Design Update	EMI request	P.44	Add PL301 Delete PJ301	20141203	DVT
8	Design Update	FAE request	P.45 P.47 P.51	Change the PC403、PC416、PC601、PC1001 from 1000P_0402_25V8J to 0.1U_0603_25V7K	20141204	DVT
9	Design Update	FAE request	P.45	Change the PC411 from 4.7U_0603_6.3V6M to 4.7U_0402_6.3V6M	20141205	DVT
10	Design Update	Solution Change	P.51	Change the PR1002 from 15K 0402 5% to 15K 0402 1% at GM Change the PR1002 from 4.7K_0402_5% to 10K_0402_1% at GT	20141215	DVT
11	Design Update	Solution Change	P.46	Change the PU501 from RT8207P to RT8207M	20150105	PVT
12	Design Update	GPU sequence fine tune RC value	P.51 P.52	GT: PR1002 change to 0 ohm and depop PC1002. GT: PR1206 change to 15k ohm.	20150119	PVT
13	Design Update	Solution Change	P.44 P.46 P.49	PQ303 change to MDV1526URH. PQ305,PQ306,PQ501 change to MDV1528URH. PQ502 change to SI7716ADN. PQ801,PQ1201,PQ1203 change to MDU1516URH. PQ802,PQ803,PQ1202,PQ1204 change to MDU1511RH.	20150119	PVT
14	Design Update	Thermal request	P.43	Change the PR216 from 16.9K to 18.2K	20150122	PVT
15	Design Update	Solution Change	P.44~47 P.49 P.51~52	Change the PR308 PR401 PR407 PR511 PR601 PR602 PR806 PR1001 PR1002 PR1201 PR1207 PR1217 PR1219 from 0ohm to R-short	20150122	PVT
16	Design Update	DFX request	P.43	Change the PJP201 footprint from ACES_50458-00801-001_8P-T to CVILU_CI9908M2HR0-NH_8P	20150122	PVT

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Version change list (P.I.R. List)

Page 1 of 2 for HW

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	35	Codec	11/10	PC Beep is digital signal	Change C2134 pin 2 connect from GNDA to GND.	DVT	0.2
2	37	USB charger	11/12	USB charger function abnormal.	Change U25 pin 4 from USB_CHARGE_2A to USB_EN Change U26 pin 4 from USB_EN to USB_CHARGE_2A	DVT	0.2
3	37	USB charger	11/17	Board ID change for DVT.	Change R506 from 0_0402_5% to 12K_0402_5%.	DVT	0.2
4	02	Block Diagram	11/19	Some block diagram descirptoin mistake.	Correct block diagram description.	DVT	0.2
5	38	EC	11/19	To solve 3V_EN need to connect to "Fixed code drive high" pin	change 3V_EN from pin 86 to 107, and original pin107 "DGPU_AC_DETECT" signal connect to EC pin 117 (NC now)	DVT	0.2
6	37	USB2.0	11/ 20	Follow EMI's request mail 1120.	Change L26 & L29 from CMMI21T-900Y-N_4P (0805 size) to MCM1012B900F06BP_4P (0504 size), and remove R458, R461, R454, R465 0_0402_5% co-lay resistors.	DVT	0.2
7	37	USB	11/ 26	JUSB3 change from bottom to top side.	Reverse JUSB3 pin connection.	DVT	0.2
8	32	LAN	11/ 27	Request by DFb	Change L2506 from SHI0000AA00 (S INDUC 2.2UH +-5% NLC252018T-2R2J-N) [2.2mm height] to SH00000RT00 (S COIL 2.2UH +-20% HPC252012NF-2R2M 1.3A) [1.2mm height]	DVT	0.2
9	39	LED	11/ 27	LED light test	Change R699 & R700 from 301_0402_1% to 470_0402_1%.	DVT	0.2
10	32	Crystal	11/ 27	Crystal EA.	Change C2558 & C2559 from 10P_0402_50V8J to 12P_0402_50V8J	DVT	0.2
11	40	Reset switch	12/ 01	RESET button 接EC_RST# or MAINPWON?	Add R2632 R-short connect to MAINPWON.	DVT	0.2
12	24, 25 26, 27	VRAM	12/ 01	fine tune VRAM	Swap U2004 & U2006 group2 connection. Swap U2008 & U2010 group4 connection.	DVT	0.2
13	40	Batt Switch	12/ 01	DFb request	Change SW4 from DE100000T00 to SN200003I00.	DVT	0.2
14	36	FFC HDD	12/ 01	FFC type HDD could pass Gen2 & Gen3 TX and iEMT EA	Add C413~C416, C538~C541 cap for co-layout without re-driver path.	DVT	0.2
15	19	NV	12/ 02	NV and EC didn't implement GPU_OVERT & GPU_ALERT code.	Change Q2000 from VGA@ to @.	DVT	0.2
16	19	NV	12/ 02	Follow NV's suggestion	1. Change D2002 & R2055 from GC6@ to @, change U2002 & R2628 from @ to GC6@. 2. Change Q2001 pin 2 & 5 from connect +3VSDGPU_MAIN to PLTRST_VGA#.	DVT	0.2
17	41	NV	12/ 03	N16V-GM not support GC6 2.0	Change J14 jumper to R2633 0_0603_5%	DVT	0.2
18	31	CRT	12/ 03	CRT EA RGB rise time fail	Change L2503 from SM01000FH00 (S SUPPRE_ MURATA BLM15BB470SN1D 0402) to SM01000LU00 (S SUPPRE_ MURATA BLM15BA220SN1D 0402)	DVT	0.2
19	35	Part Reference	12/ 03	Correct part referernce type	Change R2120~R2123 to L2511~L2514	DVT	0.2

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21	17	Test	12/05	Test plan	Reserve Q2007 , place close to U45.	DVT	0.2
22	10	Test	12/05	Test plan	Reserve R2634 , place close to U30.	DVT	0.2
23	13,17	DRAM	12/10	Choose cap. for better placement.	Depop C18, pop C118.	DVT	0.2
24	39	Lid SW	12/10	Change main source.	Change U4 PN to SA00008K800.	DVT	0.2
25	37	USB20 choke	12/17	SM070003K00 will shift when SMT and prohibit by factory.	Change L26 & L29 to SM070003Y00.	DVT	0.2
26	19	NV	12/17	To prevent could not read or read wrong graphic temperature via I2C and cause over temperature.	Add Q2000 to let GPU_OVERT work.	DVT	0.2
27	19	NV	12/17	VGA_PWROK pull high to +3VS via 10K ohm, but R2014 10K pull down will make VGA_PWROK high voltage level out of spec.	Change R2014 from 10K to 200K ohm. (Follow NV reference schematic.)	DVT	0.2
28	38	Board ID	12/22	Change board ID for PCB Revision 0.3	Change R506 from SD028120280 12K ohm to SD028150280 15K ohm	PVT	1.0
29	13, 17	POS Cap	12/22	Follow schematic design common rule, POS Cap should use Serial P/N	Change C18 & C118 from SGA20331E10 to SGA00009500	PVT	1.0
30	39	ON/OFF button	12/30	SW6 is for RD test at NPI phase only.	Change SW6 from DB@ to @.	PVT	1.0
31	39	LED	12/30	LED test with DVT ME module.	Change R699 & R700 from 470 ohm (SD034470080) to 560 ohm (SD000008380) Change R698 & R701 from 390 ohm (SD00000QZ00) to 430 ohm (SD00000LM00)	PVT	1.0
32	19	NV	12/30	GPU throttle test.	Reserve U17 for test.	PVT	1.0
33	39	NV	12/30	Reserve level shift circuit to prevent Elan touch pad back drive issue.	Reserve Q2008, R2640~R2642 level shift circuit.	PVT	1.0
34		Component	1/7	Follow standard part	Change Q7, Q8, Q14, Q15, Q40, Q1007, Q2000, Q2001, Q2003, Q2004, Q2008 from SB00000DH00 (S TR DMN66D0LDW-7 2N SOT363-6) to SB00000PV00 (S TR L2N7002DW1T1G 2N SC88-6)	PVT	1.0
35	36	Test	1/8	Reserve G-SEN_INT2 connector to JHDD2.	Reserve R2643 & R2644.	PVT	1.0
36	34	WLAN	1/12	SUSCLK will back drive to +3VS_WLAN when S3 or S5 with Broadcom NFA435 module. Check module datasheet not support SUSCLK, and intel module could define as NC.	Change R2612 from R-short to non-pop.	PVT	1.0
37	40	Screw hole	1/12	ME change NGFF standoff hole from 3.2 change to 3.3mm	Change H17 Footprint from H_3P2 to H_3P3.	PVT	1.0
38	35	Codec	1/19	ALC255 have PC beep in detect ciucuit in chip. Signal level under 400mV will disable PC Beep function.	Change R2140 from SD028470280 (47K_0420_5%) to SD028270280 (27K_0402_5%)	PVT	1.0
39	41	NV	1/19	To meet N16S-GT power sequence	Add virtual symbol R469 for SGT@, change vaule from 47K_0402_5% to 20K_0402_5%. Original R469 change from VGA@ to VGM@.	PVT	1.0
40	37	USB Charger	1/19	USB charger CB pin need a dedicate pin to control behavior.	Change USB charger CB control pin from SUSP# to USB_CHARGE_CB connect to EC pin 86.	PVT	1.0
41	18	ESD	1/21	ESD Jason request to reserve a cap for DIMM_DRAMRST#.	Reserve C2611.	PVT	1.0

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